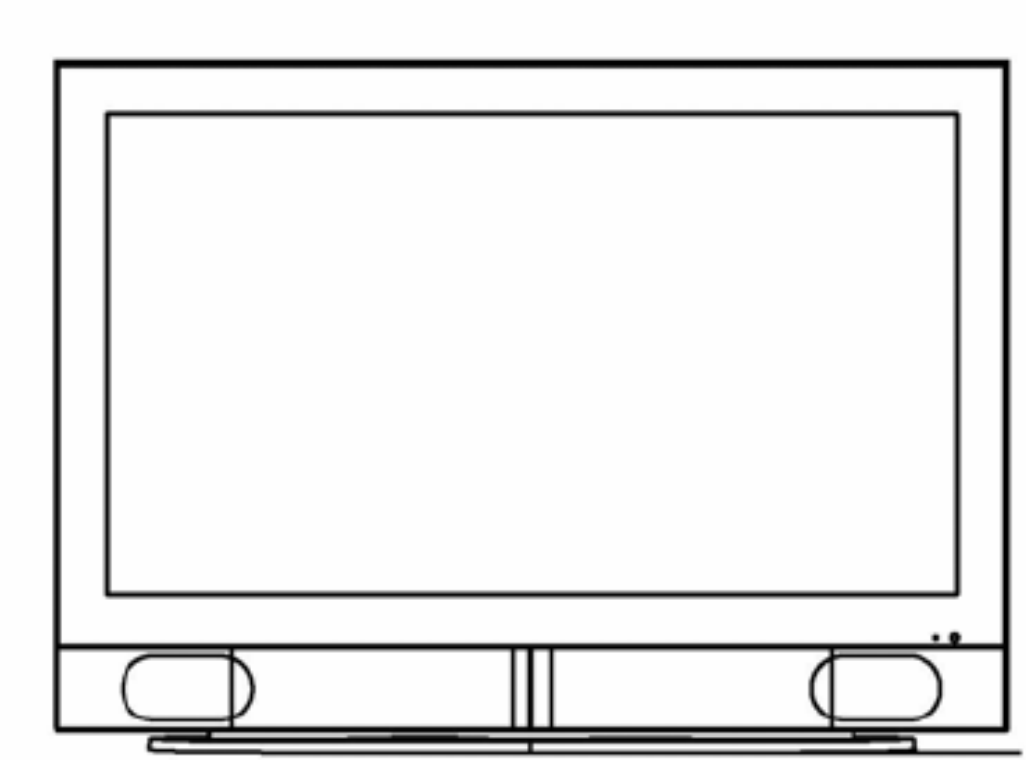
Service Manual



Model #: VIZIO L42HDTV10A

VIZIO GV42L HDTV

V, Inc

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Top Confidential

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FCC INFORMATION
This equipment has been tested and found to comply with the limits of a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that the interference will not occur in a particular installation. If this equipment does cause unacceptable interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures -- reorient or relocate the receiving antenna; increase the separation between equipment and receiver; or connect the into an outlet on a circuit different from that to which the receiver is connected.

FCC WARNING
To assure continued FCC compliance, the user must use a grounded power supply cord and the provided shielded video interface cable with bonded ferrite cores. Also, any unauthorized changes or modifications to Amtrak products will void the user’s authority to operate this device. Thus VINC Will not be held responsible for the product and its safety.

CE CERTIFICATION
This device complies with the requirements of the EEC directive 89/336/EEC with regard to “Electromagnetic compatibility.”

SAFETY CAUTION
Use a power cable that is properly grounded. Always use the AC cords as follows – USA (UL); Canada (CSA); Germany (VDE); Switzerland (SEV); Britain (BASEC/BS); Japan (Electric Appliance Control Act); or an AC cord that meets the local safety standards.

Chapter 1 Features

1. Built in TV channel selector for TV viewing.

2. Simulatnueous display of PC and TV images.

3. Connectable to PC's analog RGB port .

4. Built in S-video, HDTV, composite video, HDMI and TV out.

5. Built in auto adjust function for automatic adjument of screen display.

6. Smoothing function enables display of smooth texts and graphics even if image withresolution lower than 1366x768 is magnified.

7. Picture In Picture (PIP) funtion to show TV or VCR images.

8. Power saving to reduce consumption power too less than 3W.

9. On Screen Display: user can define display mode (i.e. color, brightness, contrast, sharpness, backlight), sound setting, PIP, TV channel program, aspect and gamma or reset all setting.

Chapter 2 Specification

1. LCD CHARACTERISTICS

Type: 42.0 WXGA TFT LCD
Size: 42.02inch
Display Size: 42.02 inches (1067.308mm) diagonal
Outline Dimension: 1006 mm (H) x 610 mm (V) x 56 mm (D) (Typ.)
Pixel Pitch: 0.227mm x 0.681mm x RGB
Pixel Format: 1366 horiz. By 768 vert. Pixels RGB strip arrangement
Contrast ratio: 1.CR : 550(Typ) 2. CR WITH AI : 1100(Typ)
Luminance, White: 500 cd/m2 (Typ)
Display Operating Mode: normally Black
Surface Treatment: Hard Coating (3H) ,Anti-glare treatment of the front polarizer.

2. OPTICAL CHARACTERISTICS

Viewing Angle (CR>10)
Left: 89°typ.
Right: 89°typ.
Top: 89°typ.
Bottom: 89°typ.

3. SIGNAL (Refer to the Timing Chart)

Sync Signal
1) Type: TMDS
2) Input Voltage Level: 90~240 Vac, 50/ 60 Hz

4.Input Connectors

RJ11, D-SUB15PIN (MINI, 3rows), Headphone, HDMIX2, RCAX3 (component), RCAX2 (AUDIO in), RCAX3 (composite), RCAX2 (AUDIO in), S-Video, Tuner

5. POWER SUPPLY

Power Consumption: 280W MAX
Power OFF: to less than 3W MAX

6.Speaker

Output 10W (max) X2

7. ENVIRONMENT

5-1. Operating Temperature: 5c~35c (Ambient)

5-2. Operating Humidity: Ta= 35 °C, 90%RH (Non-condensing)

5-3. Operating Altitude: 0 - 14,000 feet (4267.2m)(Non-Operating)

8. DIMENSIONS (Physical dimension)

Width: 1066 mm.

Depth: 269.2mm

Height: 765.4mm

9. WEIGHT (Physical weight)

a. Net: 36.0+/-0.5kgs

b. Gross: 43+/-0.5kgs

9-1. MOUNTING PRECAUTIONS

(1) You must mount a module using holes arranged in four corners or four sides.

(2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.

(3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.

(4) You should adopt radiation structure to satisfy the temperature specification.

(5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.

(6) Do not touch, push or rub the exposed polarizes with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)

(7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.

(8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.

(9) Do not open the case because inside circuits do not have sufficient strength.

9-2. OPERATING PRECAUTIONS

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage : V=±200mV(Over and under shoot voltage)

(2) Response time depends on the temperature. (In lower temperature, it becomes longer.)

(3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)And in lower temperature, response time (required time that brightness is stable after turned on) becomes longer.

(4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.

(5) When fixed patterns are displayed for a long time, remnant image is likely to occur.

(6) Module has high frequency circuits. System manufacturers shall do sufficient suppression to the electromagnetic interference. Grounding and shielding methods may be important to minimize the interference.

9-3. HANDLING PRECAUTIONS FOR PROTECTION

(1) The protection film is attached to the bezel with a small masking tape. When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.

(2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the bezel after the protection film is peeled off.

(3) You can remove the glue easily. When the glue remains on the bezel surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

Chapter 3 On Screen Display

Main unit button

Power

MENU

CH ▲

CH ▼

VOL +

VOL -

Input

TV Source

A. Picture Adjust：

a. Picture Mode (Standard/Movie /Game / Custom)

b. Backlight (0~100)

c. Contrast (0~100)

d. Brightness (0~100)

e. Color (saturation)(0~100)

f. Tint (hue) (0~100)

g. Sharpness (0~7)

h. Color Temperature (Cool/Normal/Warm/Custom)

i. Advanced Picture Adjust

B. Audio Adjust：

a. Volume (0~100)

b. Bass (0~100)

c. Treble (0~100)

d. Balance (0~100)

e. Surround (ON/OFF)

f. Speakers (ON/OFF)

C. Special Features：

a. Language (English/Français/Espaňol)

b. Sleep Timer (OFF/30Min/60Min/90Min/120Min)

c. Analog CC (OFF/CC1~4/TT1~4)

d. Digital CC (OFF/CC1~4/Service1~6)

e. Digital CC Style

f. PIP Position (TL/TC/TR/ML/MR/BL/BC/BR)

g. Rest All Setting

D. TV Tuner Setup：

a. Tuner Mode (Cable/Air)

b. Auto Search

c. Skip Channel

d. Digital Audio Out (PCM/Dolby Digital)

e. Time Zone
(Eastern/Indiana/Central/Mountain/Arizona/Pacific/Alaska/Hawaii)

E. Parental Control：

a. Parental Lock Enable (ON/OFF)

b. TV Rating

c. Move Rating

d. Block Unrated TV (NO/Yes)

e. Access Code Edit

RGB Mode

A. Picture Adjust：

a. Auto Adjust

b. Backlight (0~100)

c. Contrast (0~100)

d. Brightness (0~100)

e. Color Temperature (9300/6300/Custom)

f. Tint (0~100)

g. H-Size (0~255)

h. Horizontal Shift (0~63)

i. Fine Tune (0~31)

B. Audio Adjust：

a. Volume (0~100)

b. Bass (0~100)

c. Treble (0~100)

d. Balance (0~100)

e. Surround (ON/OFF)

f. Speakers (ON/OFF)

C. Special Features：

a. Language (English/Français/Espaňol)

b. Sleep Timer (OFF/30Min/60Min/90Min/120Min)

c. PIP Position (TL/TC/TR/ML/MR/BL/BC/BR)

d. Rest All Setting

AV COMPONENT MODE

A. Picture Adjust：

a. Picture Mode (Standard/Movie /Game / Custom)

b. Backlight (0~100)

c. Contrast (0~100)

d. Brightness (0~100)

e. Color (saturation)(0~100)

f. Tint (hue) (0~100)

g. Sharpness (0~7)

h. Color Temperature (Cool/Normal/Warm/Custom)

i. Advanced Picture Adjust

B. Audio Adjust：

a. Volume (0~100)

b. Bass (0~100)

c. Treble (0~100)

d. Balance (0~100)

e. Surround (ON/OFF)

f. Speakers (ON/OFF)

C. Special Features：

a. Language (English/Français/Espaňol)

b. Sleep Timer (OFF/30Min/60Min/90Min/120Min)

c. Analog CC (OFF/CC1~4/TT1~4)

d. PIP Position (TL/TC/TR/ML/MR/BL/BC/BR)

e. Rest All Setting

D. Parental Control：

a. Parental Lock Enable (ON/OFF)

b. TV Rating

c. Move Rating

d. Block Unrated TV (NO/Yes)

e. Access Code Edit

HDMI MODE：

A. Picture Adjust：

a. Picture Mode (Standard/Movie /Game / Custom)

b. Backlight (0~100)

c. Contrast (0~100)

d. Brightness (0~100)

e. Color (saturation)(0~100)

f. Tint (hue) (0~100)

g. Sharpness (0~7)

h. Color Temperature (Cool/Normal/Warm/Custom)

i. Advanced Picture Adjust

B. Audio Adjust：

a. Volume (0~100)

b. Bass (0~100)

c. Treble (0~100)

d. Balance (0~100)

e. Surround (ON/OFF)

f. Speakers (ON/OFF)

C. Special Features：

a. Language (English/Français/Espaňol)

b. Sleep Timer (OFF/30Min/60Min/90Min/120Min)

c. PIP Position (TL/TC/TR/ML/MR/BL/BC/BR)

d. Rest All Setting

Chapter4 Factory preset timings

This timing chart is already preset for the TFT LCD analog & digital display monitors.

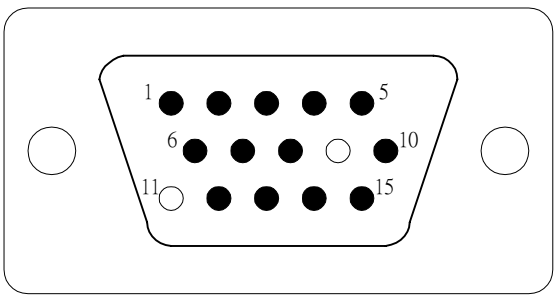
Resolution	Refresh rate	Horizontal Frequency	Vertical Frequency	Horizontal Polarity	Vertical Polarity	Pixel Rate
640x480	60Hz	31.5kHz	59.94Hz	N	N	25.175
640x480	75Hz	37.5kHz	75.00Hz	N	N	31.500
800X600	60Hz	37.9kHz	60.317Hz	P	P	40.000
800x600	75Hz	46.9kHz	75.00Hz	P	P	49.500
800X600	85Hz	53.7kHz	85.06Hz	P	P	56.250
1024x768	60Hz	48.4kHz	60.01Hz	N	N	65.000
1024X768	75Hz	60.0kHz	75.03Hz	P	P	78.750
720x400	70Hz	31.46kHz	70.08Hz	N	P	28.320
1366X768	60	47.7KHZ	60.00HZ	P	N	85.500

Remark: P: positive N: negative

Chapter 5 Pin Assignment

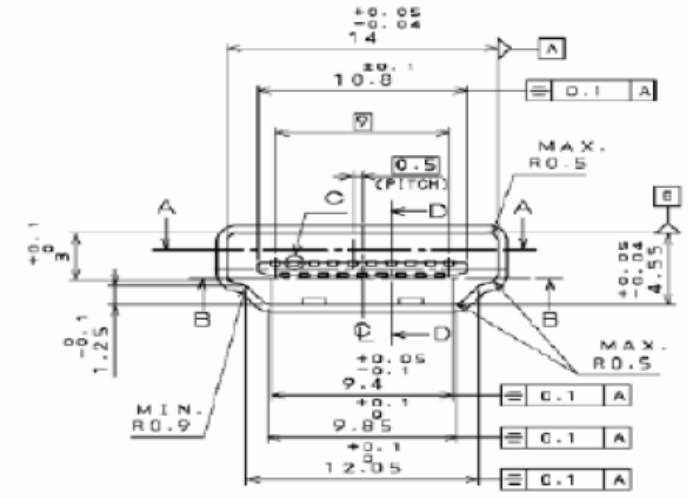
The TFT LCD analog display monitors use a 15 Pin Mini D-Sub connector as video input source.

Pin	Description
1	Red
2	Green
3	Blue
4	Ground
5	Ground
6	R-Ground
7	G-Ground
8	B-Ground
9	+5V for DDC
10	Ground
11	No Connection
12	(SDA)
13	H-Sync (Composite Sync)
14	V-Sync
15	(SCL)



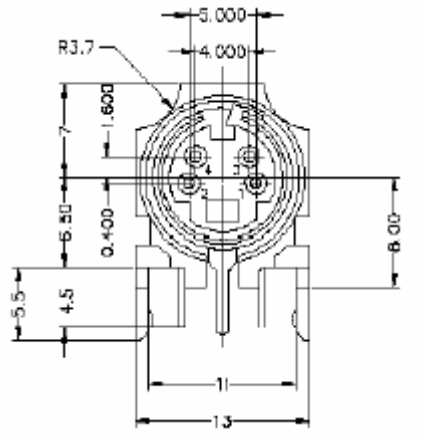
HDMI CONNECT PIN ASSIGNMENT

PIN	SIGNAL ASSIGNMENT
1	TMDS Data2+
2	TMDS Data2 Shield
3	TMDS Data2-
4	TMDS Data1+
5	TMDS Data1 Shield
6	TMDS Data1-
7	TMDS Data0+
8	TMDS Data0 Shield
9	TMDS Data0-
10	TMDS Clock+
11	TMDS Clock Shield
12	TMDS Clock-
13	CEC
14	Reserved (N.C on device)
15	SCL
16	SDA
17	DDC/CEC Ground
18	+5V Power
19	Hot Plug Detect



Four-Pin mini DIN S-Video Connector

a. Pin Assignment



b. Signal Level Video (Y): Analog 0.1Vp-p/75Ω

Video (C): Analog 0.286p-p/75

Sync (H+V): 0.3V below Video (Y)

c. Frequency H: 15.734KHz V: 60Hz (NTSC)

Signal Level Video (Y) : Analog 0.1Vp-p/75Ω

Video (C) : Analog 0.286p-p/75Ω

Sync (H+V): 0.3V below Video (Y)

Frequency H: 15.734Khz V: 60HZ (NTSC)

F-Type TV RF connector

a. Signal Level 60dBμV typical

b. System NTSC

c. Frequency 55~801MHz (NTSC)

PC connector 15 pin male D-sub connector

a. Pin Assignment Refer to Section 2.3.10

b. Signal Level Video (R, G, B): Analog 0.7Vp-p/75Ω

Sync (H, V): TTL level

RGB Signal:

a. Sync Type TTL (Separate / Composite) or Sync. On Green

b. Sync polarity Positive or Negative

c. Video Amplitude RGB: 0.7Vp-p

d. Frequency H: support to 30K~70KHz

V: support to 50~85Hz

Pixel Clock: support to 110MHz

HDMI Signal (HDMI):

a. Pin Assignment Refer to HDNI Pin Assignment

b. Type A

c. Polarity Positive or Negative

d. Frequency

H: 15.734KHz V: 60Hz (NTSC-480i)

H: 31KHz V: 60Hz (NTSC-480p)

H: 45KHz V: 60Hz (NTSC-720p)

H: 33KHz V: 60Hz (NTSC-1080i)

Component signal (Component 1 and Component 2)

Component 1

a. Frequency H: 15.734KHz V: 60Hz (NTSC-480i)

H: 31KHz V: 60Hz (NTSC-480p)

H: 45KHz V: 60Hz (NTSC-720p)

H: 33KHz V: 60Hz (NTSC-1080i)

b. Signal level Y: 1Vp-p Pb: ±0.350Vp-p Pr: ±0.350Vp-p

c. Impedance 75Ω

Component 2

a. Frequency H: 15.734KHz V: 60Hz (NTSC-480i)

H: 31KHz V: 60Hz (NTSC-480p)

H: 45KHz V: 60Hz (NTSC-720p)

H: 33KHz V: 60Hz (NTSC-1080i)

b. Signal level Y: 1Vp-p Pb: ±0.350Vp-p Pr: ±0.350Vp-p

c. Impedance 75Ω

Chapter 6 Main Board I/o Connections

J6 CONNECTION (TOP→BOTTOM)

Pin	Description
1	“+5V”
2	“+3.3V”
3	“ADCKEY”
4	“LED”
5	“PWR KEY”
6	“GND”
7	“GND”
8	“IR”

J7 CONNECTION (TOP→BOTTOM)

Pin	Description
1	“POWRSW”
2	“+12V”
3	“+12V”
4	“+12V”
5	“GND”
6	“GND”
7	“GND”
8	“GND”
9	“GND”
10	“+5V”
11	“+5V”
12	+5V
13	“PWM”
14	“BL ON/OFF”

Chapter 7 Theory of Circuit Operation

The operation of D-SUB 15pin route

The D-SUB 15pin is input analog signal to the MTK8202 transfer A/D converter then generates the vertical and horizontal timing signals for display device.

The operation of HDMII CON route

The HDMI 1&2 CON is input digital signal to the PI3HDMI412FT switch output signal is process to the MT8293. Then transfer to the MTK8202, the MTK8202 generates the vertical and horizontal timing signals for display device.

The operation of HDTV & Component route

HDTV & Component signal is input to the MTK8202 then MTK8202 generates the vertical and horizontal timing signals for display device.

The operation of Video 1,2,3 & S-Video route

The Video 1,2 and S-Video signal is transmission signal to the MTK8202 then MTK8202 generates the vertical and horizontal timing signals for display device.

The operation of TV route

TV signal is processes to the tuner and output to MTK8202 then MTK8202 generates the vertical and horizontal timing signals for display device. Audio is processes to the tuner output to SIF circuit and output to MTK8202.Then MTK8202 process to wm8776 and output to TDA8946J transfer to speaker

The operation of DTV route

DTV signal is processes to the tuner and transmission to MT5112 and output signal to MT5351 then MT5351 output to MT8202 generates the vertical and horizontal timing signals for display device.

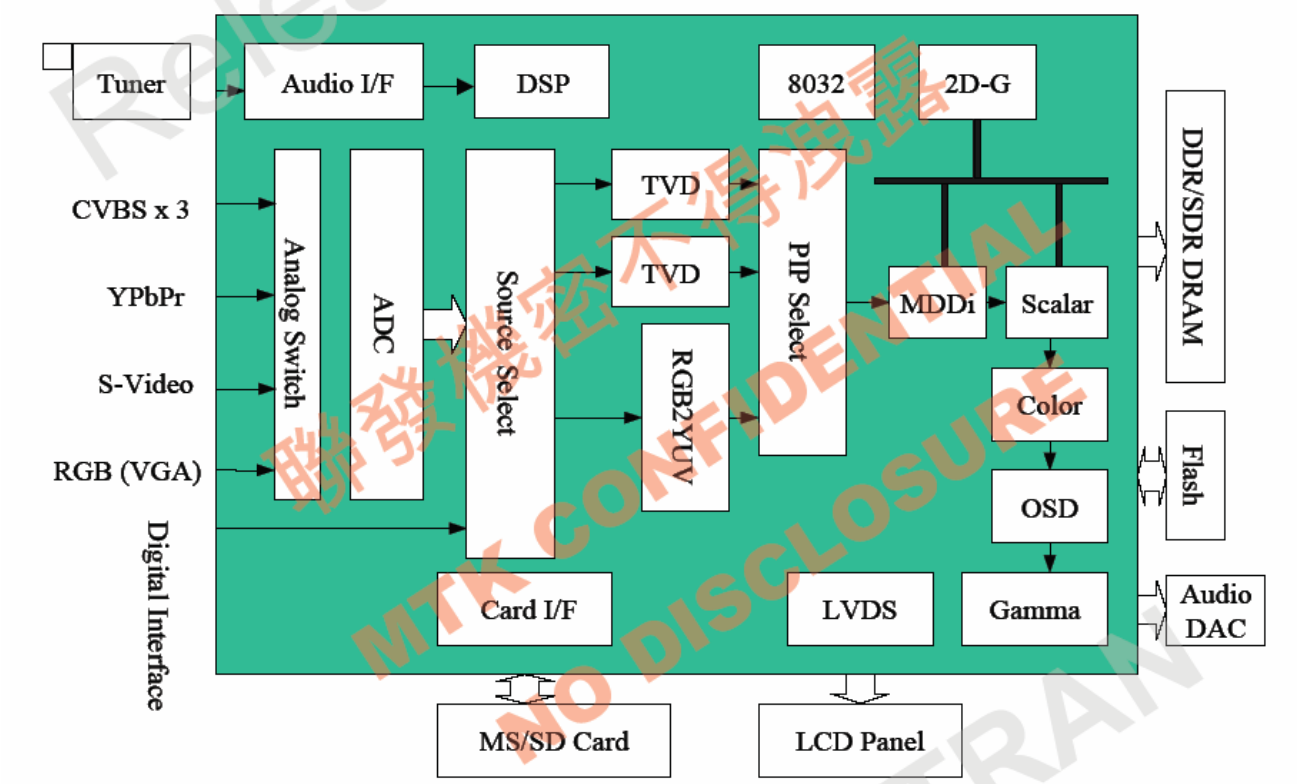
The operation of keypad

There are 7 keys to control and select the function of L42 and also has one LED to indicate the status of operation. They are “Power, ▼▲, + -, Input, OSD”.

MT8202 Application

MT8202 is a highly integrated video and audio single chip processor for emerging HDTV-Ready LCD TV. It includes one 3D/2D TV Decoder recovering the best image from CVBS, and in addition, its analog input also support popular S-Video, Component, VGA video source. On-chip advanced motion adaptive de-interlacer (MDDitm) converts accordingly the interlace video into smooth non-flicking progressive motion pictures. With on-chip advanced 2D Graphic processor,MT8202 provides customers with high quality UI adding significant end product value. Flexible scalar provides wide adoption to various LCD panel for different video sources. Its on-chip audio processor decodes whole world standard audio signals from tuner with lip sync control, delivering high quality post-processed sound effect to customers. On-chip microprocessor and reference FW reduces the system BOM and shortens the schedule of UI design by high-level C program. With truly SOC design, MT8202 offers our customers the real cost-effective high performance HDTV-ready solution.

BOLOCK DIAGRAM



1. Video input

a. Input Multiplexing

1.component X2

2.composite X2

3.s-videoX1

4.HDMI X2

5.VGA X1

6.RF&DTV X1

b. Input formats:

1.support HDTV 480i/480p/720p/1080p

2.support Y/C signal 1VP-P/75Ω

3.support Y/C signal 1VP-P/75Ω

4.support 480i/408p/720p/1080i/1080p

5.support VGA input up to 1366x168@60HZ

6.support RF NTSC system Frequency 55~801MHZ;DTV 480i/480p/720p/1080p

2. Decoder

TVD

1.Single 2nd generation TV decoder

2.Automatic TV standard detection supporting NTSC, NTSC-4.43, PAL (B, G, D, H, M, N, I, Nc), PAL (Nc), PAL, SECAM

3.Enhanced 2nd generation NTSC/PAL Motion Adaptive 3D comb filter

4.Motion Adaptive 3D Noise Reduction

5.Embedded VBI decoder for Closed-Caption/XDS/ Teletext/WSS/VPS

6.Supporting Macro vision detection

YPbPr/Scart/D-connector

1.Supporting HDTV 480i/480p/576i/576p/720p/1080i input

2.Smart detection on Scart function for European region

3.Smart detection on D-connector for Japan region

4.Supporting SCART RGB inputs mixed with composite signal by adjustable horizontal delay

VGA

1.Supporting various VGA input timings up to SXGA (1280x1024@75Hz).

2.Supporting Separate/Composite/SOG sync types

Digital port

1.1 digital port supporting DVI 24-bit RGB or CCIR-656/601 digital video input format

2.1 additional 8 bit digital port for ITU656 video format

VBI

1.Dual VBI decoders for the application of V-Chip/Closed-Caption/XDS/ Teletext/WSS/VPS

2.Supporting external VBI decoder by YPrPb input

3.VBI decoder up to 1000 pages Teletext.

3. Support Formats:

Support NTSC, NTSC-4.43

Automatic Luma / Chroma gain control

Automatic TV standard detection

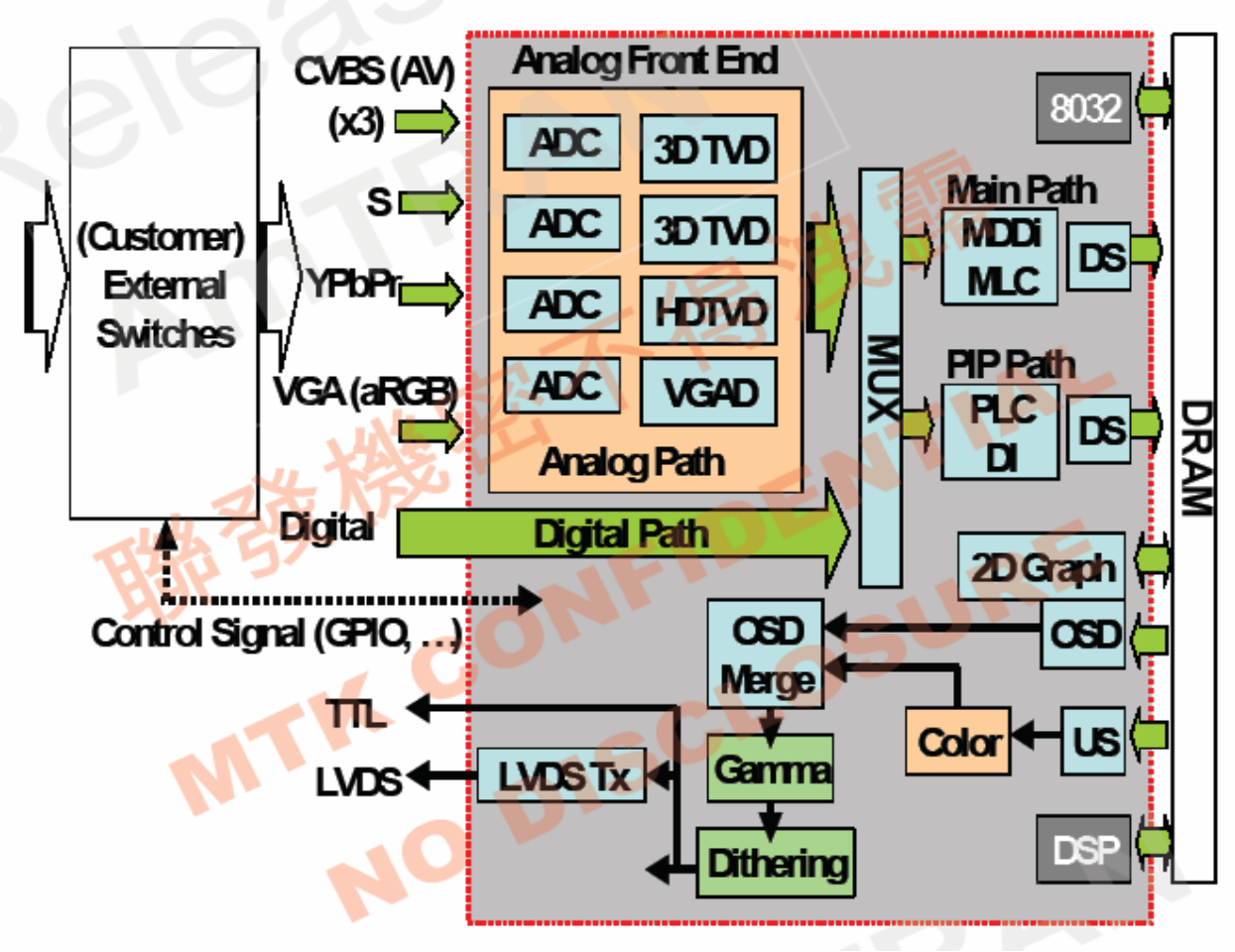
NTSC Motion Adaptive 3D comb filter

Motion adaptive 3D Noise Reduction

VBI decoder for closed-caption/XDS/Teletext/WSS/VPS

Macro vision detection

BOLOCK DIAGRAM



4. 2D-Graphic/OSD processor

Embedded two backend RGB domain OSD planes and one YUV domain OSD plane. to support Main/PIP Teletext/Close-caption functions together with setup menu

1.Supporting alpha blending among these two planes and video

2.Supporting Text/Bitmap decoder

3.Supporting line/rectangle/gradient fill

4.Supporting bitblt

5.Supporting color Key function

6.Supporting Clip Mask

7.65535/256/16/4/2-color bitmap format OSD,

8.Automatic vertical scrolling of OSD image

9.Supporting OSD mirror and upside down

5. Microprocessor interface

When power is supplied and power key is pressed then the rest circuit lets Reset to low state that will reset the MTK8202 to initial state. After that the Reset will transits to high state and the MTK8202 start to work that microprocessor executes the programs and configures the internal registers. The execution speed of CPU is 162 MHz.

1. The I/O ports are configured as follows：

Pin name	Function	Type	Description
AD17	PWM	Output	Backlight Adjust
R3	GPIO2	Output	Panel on/off
V1	GPIO7	Output	System power
Y2	GPIO16	Output	LVDS on/off
R4	GPIO3	Output	ATSC POW on/off
AD22	IOSCL	Input / Output	SDA
AV22	IOSDA	Input / Output	SCL
W3	GPIO13	Output	HDMI Switch Select
Y4	GPIO_18	Output	MT8293 Reset
W4	GPIO_14	Output	MT8293 acknowledge to player
B19	ADC_IN0	Input	Key ADC detection
L4	IR	Input	IR Receiver
Y1	GPIO_15	Output	SYSTEM EEPROM Read / Write
T2	GPIO_23	Output	LED Backlight
L2	RESETn	Input	MT8202 RESET
R2	GPIO_1	Output	DTV & HDMI Select PIN
T4	GPIO_4	Output	DTV & ATV Select PIN

2. PIP/POP HARDWARE LIMITION:

MAIM/PIP TABLE (8202)							
PIP / MAIN	TV	ATSC (DTV)	AV1	AV2/S-VIDEO	COMPONENT 1&2	HDMI 1&2	PC
TV		X	X	X	O	O	O
ATSC (DTV)	X		X	X	O	X	O
AV1	X	X		X	O	O	O
AV2/ S-VIDEO	X	X	X		O	O	O
COMPONENT 1&2	O	O	O	O		O	X
HDMI 1&2	O	X	O	O	O		O
PC	O	O	O	O	X	O	

6. Video processor

1.Color Management

Fully 10-bit processing to enhance the video quality

Advanced flesh tone and multiple-color enhancement. (For skin, sky, and grass…)

Gamma/anti-Gamma correction

Advanced Color Transient Improvement (CTI)

Saturation/hue adjustment

2.Contrast/Brightness/Sharpness Management

Sharpness and DLTI/DCTI

Brightness and contrast adjustment

Black level extender

White peak level limiter

Adaptive Luma/Chroma management

3.De-interlacing

2nd generation advanced Motion adaptive de-interlacing

Automatic detect film or video source

3:2/2:2 pull down source detection

Main/PIP 2 independent de-interlacing processor

4.Scaling

2nd generation high resolution arbitrary ratio vertical/horizontal scaling of video, from 1/32X to 32X

Advanced linear and non-linear Panorama scaling

Programmable Zoom viewer

Picture-in-Picture (PIP)

Picture-Out-Picture (POP)

5.Display

Advanced dithering processing for LCD display with 6/8/10 bit output

10bit gamma correction

Supporting alpha blending for Video and two OSD planes

Frame rate conversion

6.Seamless performance comparing demonstration function

Support Left/Right video processing comparing function without additional resources (DRAM…) for customers' demonstration

All the video functions (De-interlace/3D comb/NR/Flesh tone/CTI) can be included

7. DRAM Usage

1.For features of 8202, Dual for enhance features support, and single 8x16 DDR for simple function support Lists are the comparison chart between function support lists of (2xDDR) and (1xDDR)

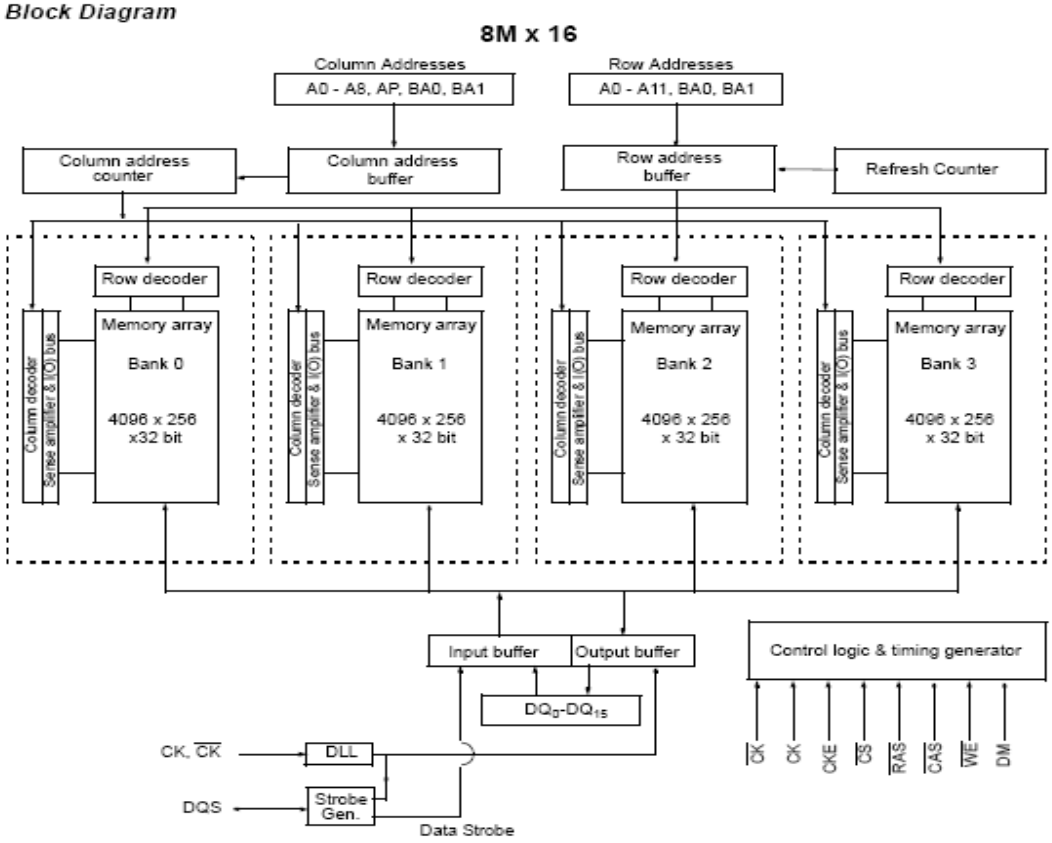
	DDR*1(16MB)	DDR*2(32MB)
NR	Y	Y
3D-Comb	Y	Y
MDDi	*480i/576i	1080i
PIP	*Y	Y
POP	*Y	Y
Display	1024x768	1366x768 1280x1024 1440x900

2.For single DDR, 8202 only support 1080i bob mode de-interlacing. (Non-3D de interlace)

3.With single DDR, it is suggested not to support PIP/POP features. Due to DDR Bandwidth limitation on PIP/POP when single DDR.

8.DDR SDRAM (V58C2128164SBI5) Application

Block Diagram



Pin description

Signal Pin Description

Pin	Type	Signal	Polarity	Function
CK $\overline{CK}$	Input	Pulse	Positive Edge	The system clock input. All inputs except DQs and DMs are sampled on the rising edge of CK.
CKE	Input	Level	Active High	Activates the CK signal when high and deactivates the CK signal when low, thereby initiates either the Power Down mode, or the Self Refresh mode.
$\overline{CS}$	Input	Pulse	Active Low	$\overline{CS}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$ $\overline{WE}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the command to be executed by the SDRAM.
DQS	Input/ Output	Pulse	Active High	Active on both edges for data input and output. Center aligned to input data Edge aligned to output data
A0 - A11	Input	Level	—	During a Bank Activate command cycle, A0-A11 defines the row address (RA0-RA11) when sampled at the rising clock edge. During a Read or Write command cycle, A0-An defines the column address (CA0-CAn) when sampled at the rising clock edge.CAn depends on the SDRAM organization: 32M x 4 DDR CAn = CA9, A11 16M x 8 DDR CAn = CA9 8M x 16 DDR CAn = CA8 In addition to the column address, A10(=AP) is used to invoke autoprecharge operation at the end of the burst read or write cycle. If A10 is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If A10 is low, autoprecharge is disabled. During a Precharge command cycle, A10(=AP) is used in conjunction with BA0 and BA1 to control which bank(s) to precharge. If A10 is high, all four banks will be precharged simultaneously regardless of state of BA0 and BA1.
BA0, BA1	Input	Level	—	Selects which bank is to be active.
DQx	Input/ Output	Level	—	Data Input/Output pins operate in the same manner as on conventional DRAMs.
DM, LDM, UDM	Input	Pulse	Active High	In Write mode, DM has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the write operation if is high for x 16 LDM corresponds to data on DQ0-DQ7, UDM corresponds to data on DQ8-DQ15.
VDD, VSS	Supply			Power and ground for the input buffers and the core logic.
VDDQ VSSQ	Supply	—	—	Isolated power supply and ground for the output buffers to provide improved noise immunity.
VREF	Input	Level	—	SSTL Reference Voltage for Inputs

Command Truth Table

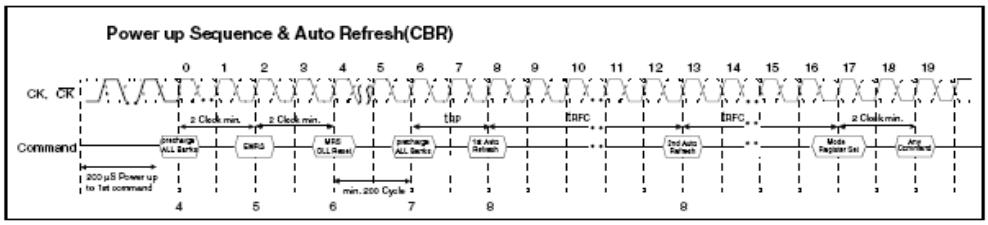
Command		CKEn-1	CKEn	CS	RAS	CAS	WE	ADDR	A10/AP	BA	Note
Mode Register Set		H	X	L	L	L	L	OP code			1,2
Extended Mode Register Set		H	X	L	L	L	L	OP code			1,2
Device Deselect		H	X	H	X	X	X	X			1
No Operation				L	H	H	H				
Bank Active		H	X	L	L	H	H	RA		V	1
Read		H	X	L	H	L	H	CA	L	V	1
Read with Autoprecharge									H		1,3
Write		H	X	L	H	L	L	CA	L	V	1
Write with Autoprecharge									H		1,4
Precharge All Banks		H	X	L	L	H	L	X	H	X	1,5
Precharge selected Bank									L	V	1
Read Burst Stop		H	X	L	H	H	L	X			1
Auto Refresh		H	H	L	L	L	H	X			1
Self Refresh	Entry	H	L	L	L	L	H	X			1
	Exit	L	H	H	X	X	X				1
				L	H	H	H				
Precharge Power Down Mode	Entry	H	L	H	X	X	X	X			1
				L	H	H	H				1
	Exit	L	H	H	X	X	X				1
				L	H	H	H				1
Active Power Down Mode	Entry	H	L	H	X	X	X	X			1
				L	V	V	V				1
	Exit	L	H	X							1

(H=Logic High Level, L=Logic Low Level, X=Don't Care, V=Valid Data Input, OP Code=Operand Code, NOP=No Operation)

1. Power-Up *Functional Description*

The following sequence is required for POWER UP.

1. Apply power and attempt to maintain CKE at a low state (all other inputs may be undefined.)
   - Apply VDD before or at the same time as VDDQ.
   - Apply VDDQ before or at the same time as VTT & Vref.
2. Start clock and maintain stable condition for a minimum of 200us.
3. The minimum of 200us after stable power and clock (CLK, CLK), apply NOP & take CKE high.
4. Precharge all banks.
5. Issue EMRS to enable DLL.(To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to all of the rest address pins, A1~A11 and BA1)
6. Issue a mode register set command for "DLL reset". The additional 200 cycles of clock input is required to lock the DLL. (To issue DLL reset command, provide "High" to A8 and "Low" to BA0)
7. Issue precharge commands for all banks of the device.
8. Issue 2 or more auto-refresh commands.
9. Issue a mode register set command to initialize device operation

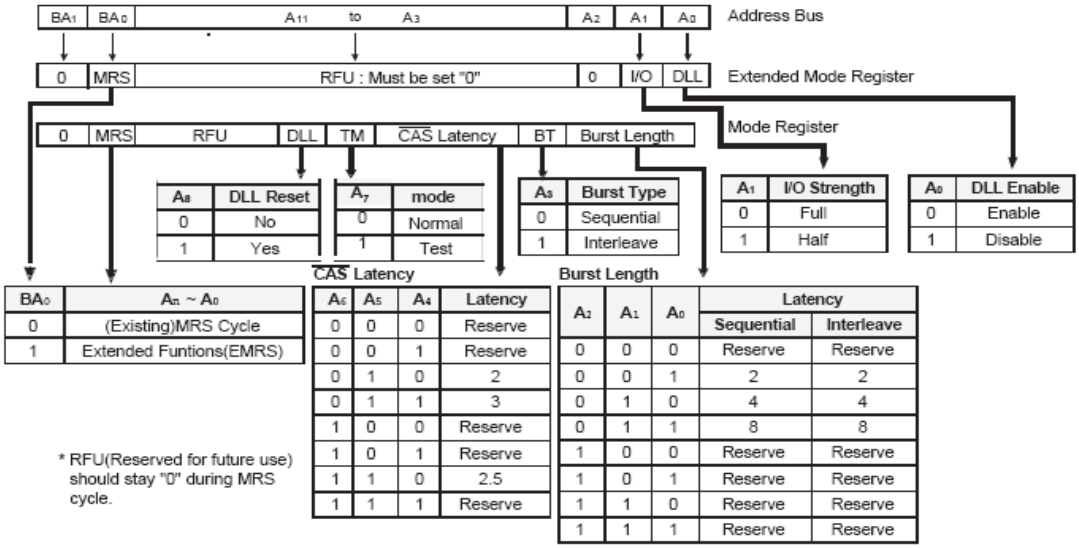


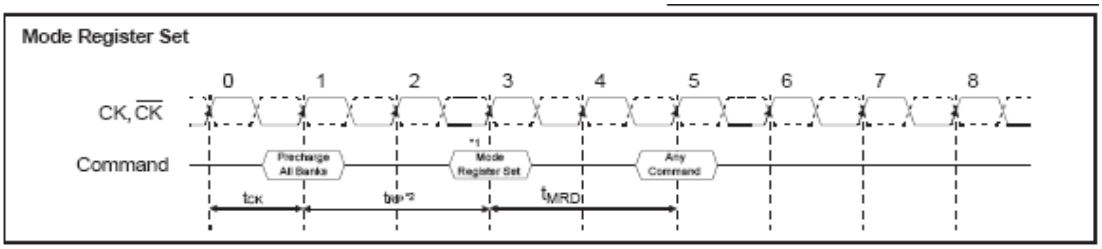
2. Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of DDR SDRAM. It programs CAS latency, addressing mode, burst length, test mode, DLL reset and various vendor specific options to make DDR SDRAM useful for a variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after EMRS setting for proper DDR SDRAM operation.

The mode register is written by asserting low on CS, RAS, CAS, WE and BA0 (The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the mode register). The state of address pins A0 ~ A11 in the same cycle as CS, RAS, CAS, WE and BA0 low is written in the mode register. Two clock cycles are required to meet tMRD spec. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A0 ~ A2, addressing mode uses A3, CAS latency (read latency from column address) uses A4 ~ A6. A7 is a ProMOS specific test mode during production test. A8 is used for DLL reset. A7 must be set to low for normal MRS operation. Refer to the table for specific codes for various burst length, addressing modes and CAS latencies.

1. MRS can be issued only at all banks precharge state.
2. Minimum tRP is required to issue MRS command.





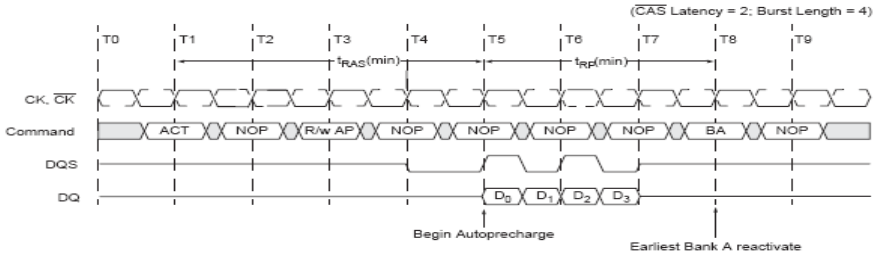
3. Precharge

The Auto Precharge operation can be issued by having column address A10 high when a Read or Write command is issued. If A10 is low when a Read or Write command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. When the Auto Precharge command is activated, the active bank automatically begins to precharge at the earliest possible moment during the Read or Write cycle once tRAS(min) is satisfied.

Read with Auto Precharge

If a Read with Auto Precharge command is initiated, the DDR SDRAM will enter the precharge operation N-clock cycles measured from the last data of the burst read cycle where N is equal to the CAS latency programmed into the device. Once the autoprecharge operation has begun, the bank cannot be reactivated until the minimum precharge time (tRP) has been satisfied.

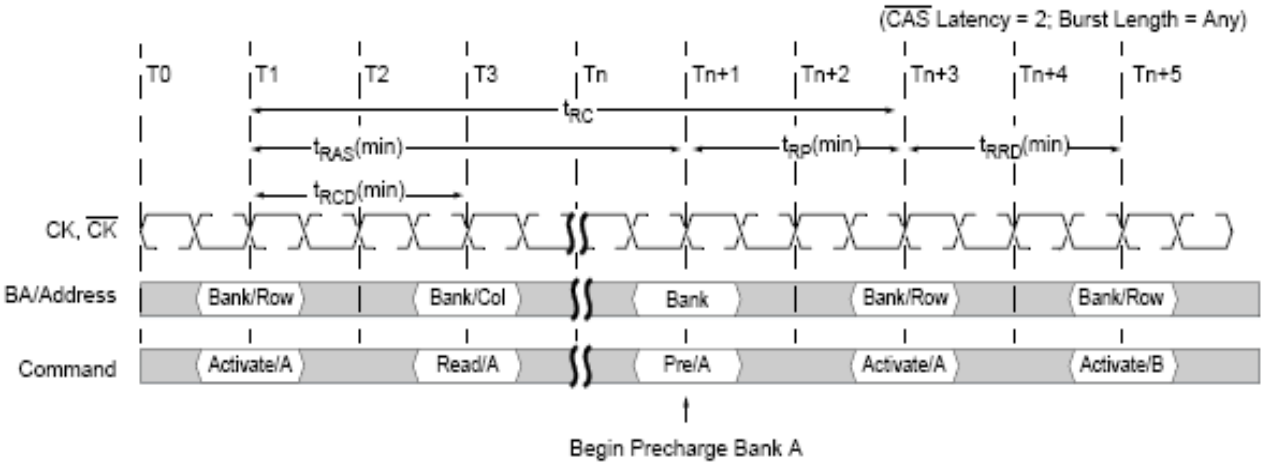
Read with Autoprecharge Timing



4. Bank Activate Command

The Bank Activate command is issued by holding CAS and WE high with CS and RAS low at the rising edge of the clock. The DDR SDRAM has four independent banks, so two Bank Select addresses (BA0 and BA1) are supported. The Bank Activate command must be applied before any Read or Write operation can be executed. The delay from the Bank Activate command to the first Read or Write command must meet or exceed the minimum RAS to CAS delay time (tRCD min). Once a bank has been activated, it must be precharged before another Bank Activate command can be applied to the same bank. The minimum time interval between interleaved Bank Activate commands (Bank A to Bank B and vice versa) is the Bank to Bank delay time (tRRD min).

Bank Activation Timing



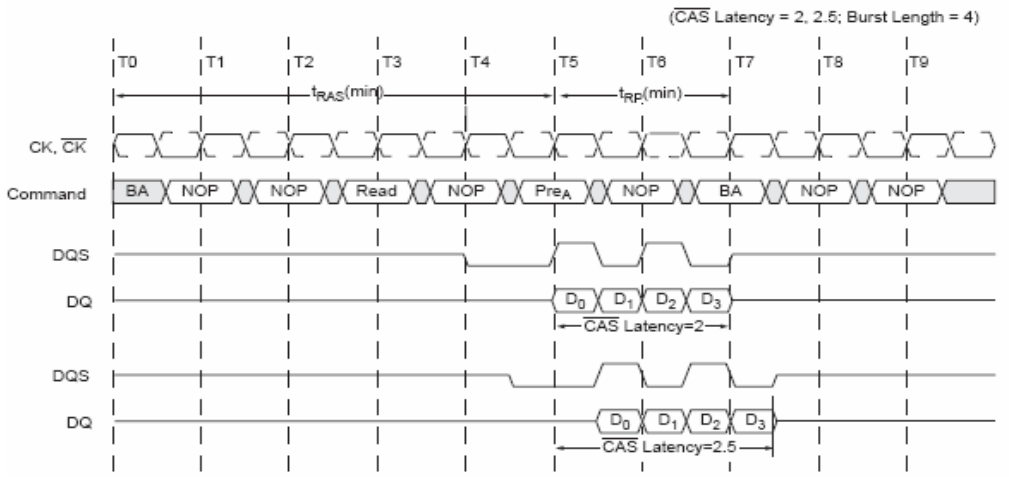
5. Read Operation

With the DLL enabled, all devices operating at the same frequency within a system are ensured to have the same timing relationship between DQ and DQS relative to the CK input regardless of device density, process variation, or technology generation. The data strobe signal (DQS) is driven off chip simultaneously with the output data (DQ) during each read cycle. The same internal clock phase is used to drive both the output data and data strobe signal off chip to minimize skew between data strobe and output data. This internal clock phase is nominally aligned to the input differential clock (CK, CK) by the on-chip DLL. Therefore, when the DLL is enabled and the clock frequency is within the specified range for proper DLL operation, the data strobe (DQS), output data (DQ), and the system clock (CK) are all nominally aligned. Since the data strobe and output data are tightly coupled in the system, the data strobe signal may be delayed and used to latch the output data into the receiving device. The tolerance for skew between DQS and DQ (tDQSQ) is tighter than that possible for CK to DQ (tAC) or DQS to CK (tDQSCK).

6. Precharge Timing During Read Operation

For the earliest possible Precharge command without interrupting a Read burst, the Precharge command may be issued on the rising clock edge, which is CAS latency (CL) clock cycles before the end of the Read burst. A new Bank Activate (BA) command may be issued to the same bank after the RAS precharge time (tRP). A Precharge command can not be issued until tRAS(min) is satisfied.

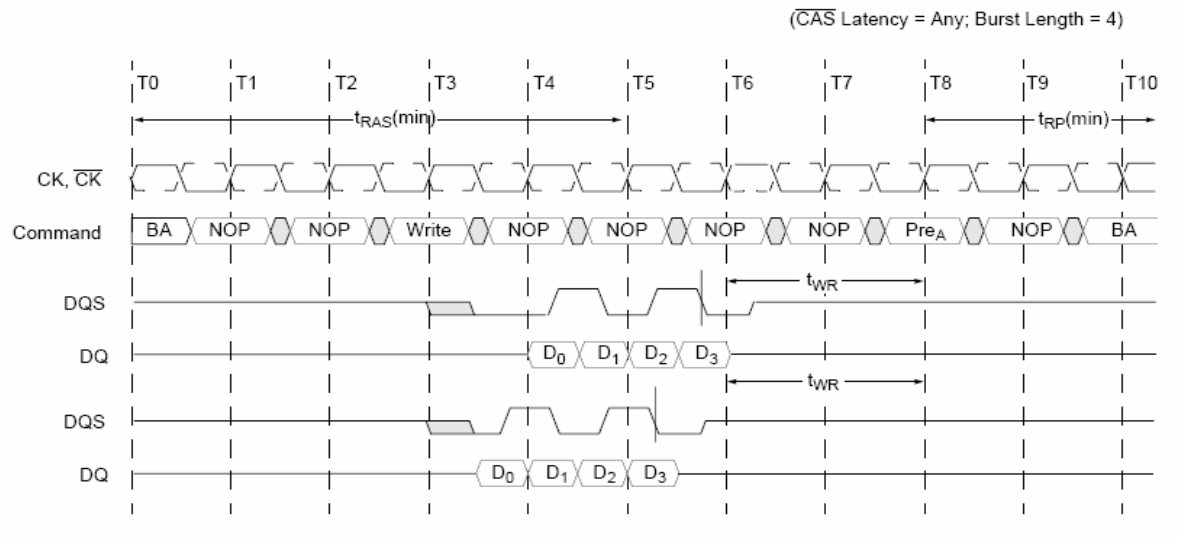
Read with Precharge Timing as a Function of $\overline{CAS}$ Latency



7.Precharge Timing During Write Operation

Precharge timing for Write operations in DRAMs requires enough time to satisfy the write recovery requirement. This is the time required by a DRAM sense amp to fully store the voltage level. For DDR SDRAMs, a timing parameter (tWR) is used to indicate the required amount of time between the last valid write operation and a Precharge command to the same bank. The “write recovery” operation begins on the rising clock edge after the last DQS edge that is used to strobe in the last valid write data. “Write recovery” is complete on the next 2nd rising clock edge that is used to strobe in the Precharge command.

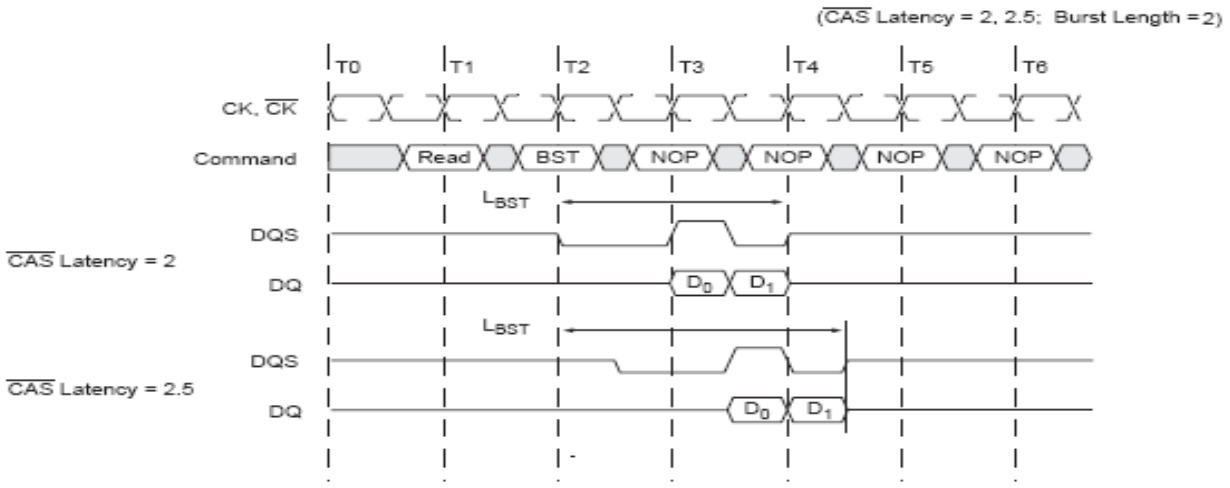
Write with Precharge Timing



8. *Burst Stop Command*

The Burst Stop command is valid only during burst read cycles and is initiated by having RAS and CAS high with CS and WE low at the rising edge of the clock. When the Burst Stop command is issued during a burst Read cycle, both the output data (DQ) and data strobe (DQS) go to a high impedance state after a delay (LBST) equal to the CAS latency programmed into the device. If the Burst Stop command is issued during a burst Write cycle, the command will be treated as a NOP command.

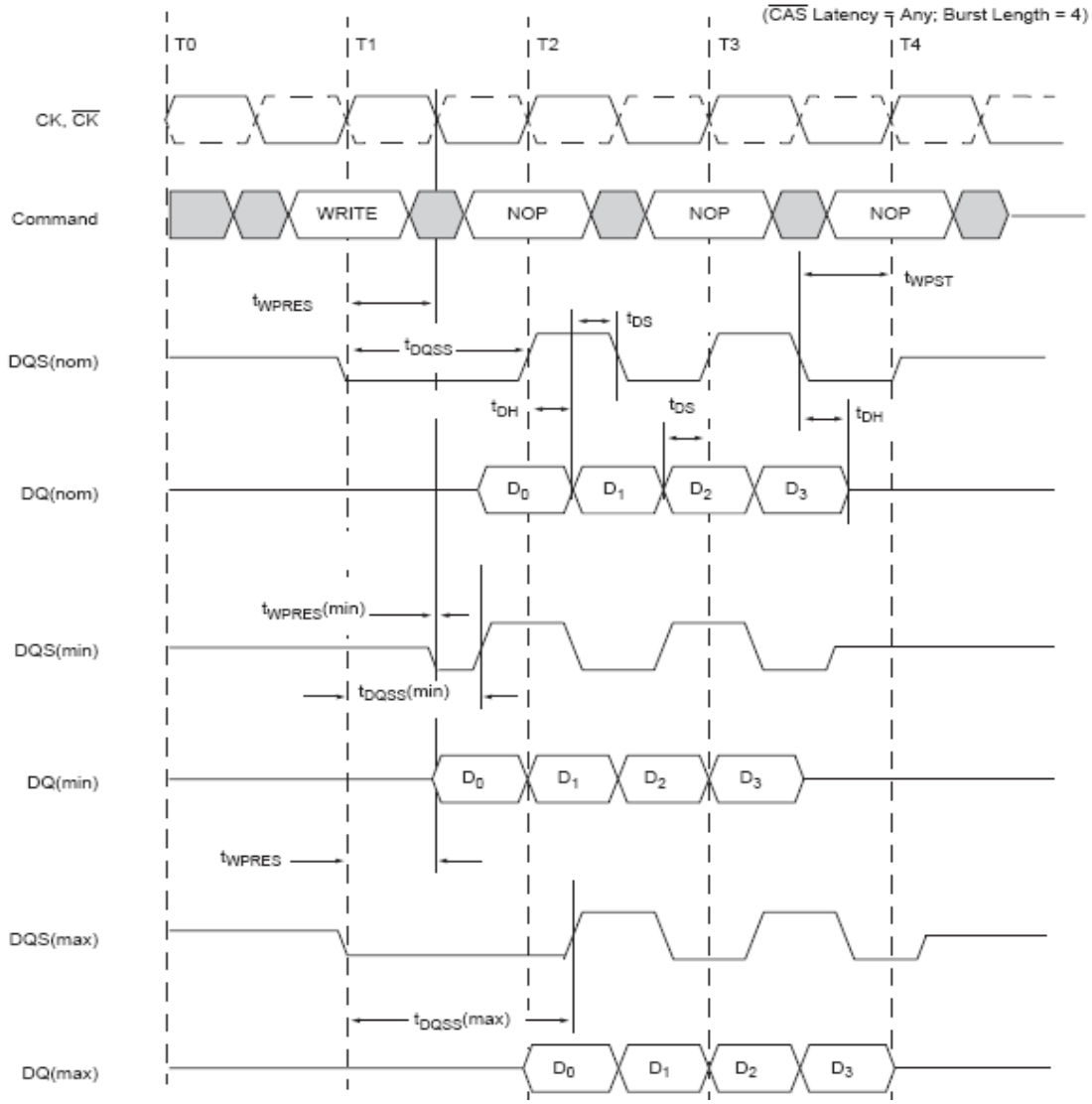
Read Terminated by Burst Stop Command Timing



9. Burst Write Operation

The Burst Write command is issued by having CS, CAS, and WE low while holding RAS high at the rising edge of the clock. The address inputs determine the starting column address. The memory controller is required to provide an input data strobe (DQS) to the DDR SDRAM to strobe or latch the input data (DQ) and data mask (DM) into the device. During Write cycles, the data strobe applied to the DDR SDRAM is required to be nominally centered within the data (DQ) and data mask (DM) valid windows. The data strobe must be driven high nominally one clock after the write command has been registered. Timing parameters tDQSS(min) and tDQSS(max) define the allowable window when the data strobe must be driven high. Input data for the first Burst Write cycle must be applied one clock cycle after the Write command is registered into the device (WL=1). The input data valid window is nominally centered around the midpoint of the data strobe signal. The data window is defined by DQ to DQS setup time (tQDQSS) and DQ to DQS hold time (tQDQSH). All data inputs must be supplied on each rising and falling edge of the data strobe until the burst length is completed. When the burst has finished, any additional data supplied to the DQ pins will be ignored.

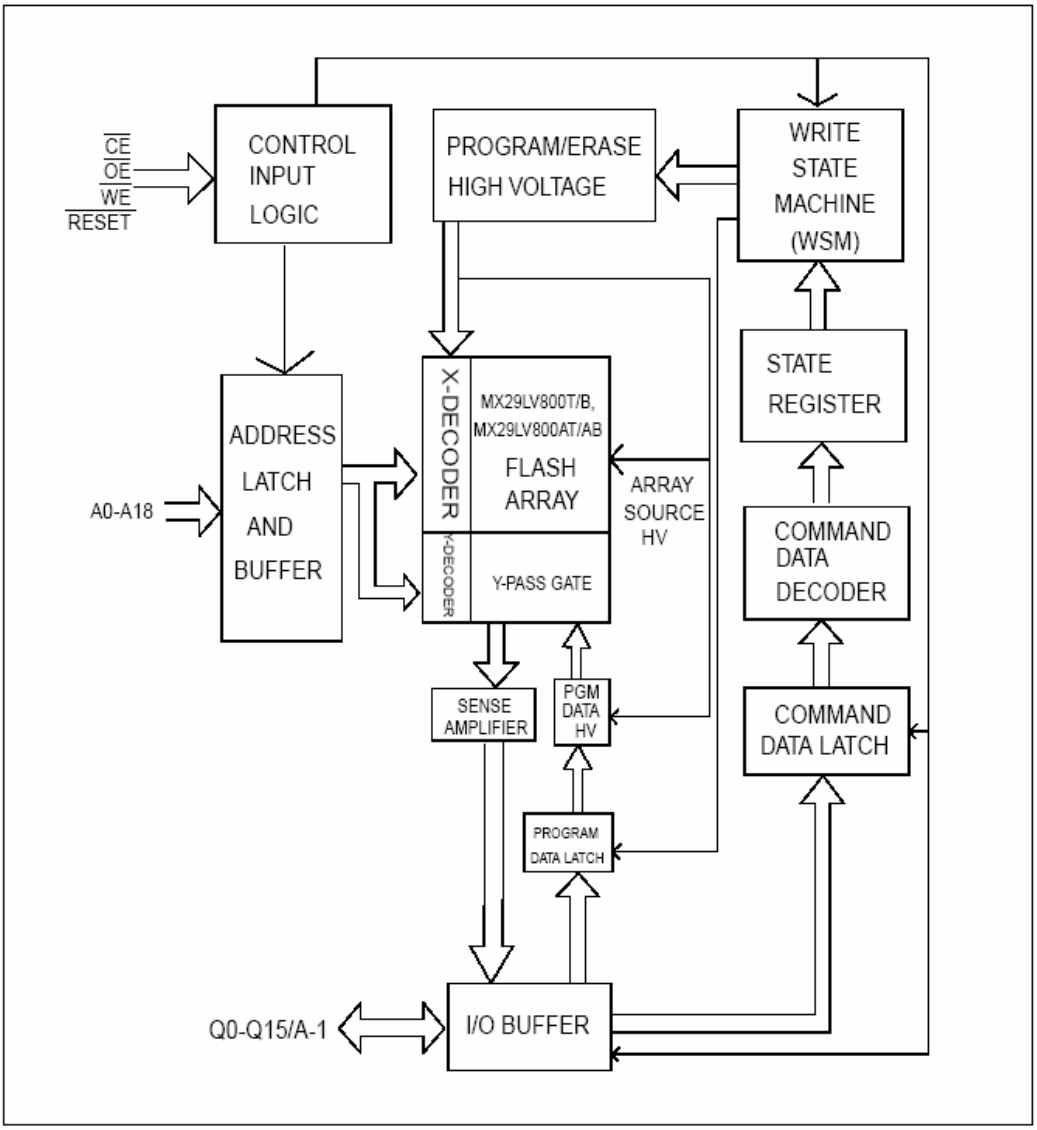
Burst Write Timing



MX29LV160BTTC (Flash) Application

The MX29LV800T/B & MX29LV800AT/AB is a 8-mega bit Flash memory organized as 1M bytes of 8 bits or 512K words of 16 bits. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX29LV800T/B & MX29LV800AT/AB is packaged in 44-pin SOP, 48-pin TSOP, and 48-ball CSP. It is designed to be reprogrammed and erased in system or in standard EPROM programmers.

BLOCK DIAGRAM



1. COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. Table 5 defines the valid register command sequences. Note that the Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress.

TABLE 6. MX29LV800T/B & MX29LV800AT/AB BUS OPERATION

DESCRIPTION	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	ADDRESS								Q0~Q7	Q8~Q15	
				A18 | A12	A10 | A11	A9	A8 | A7	A6	A5 | A2	A1	A0		BYTE =VIH	BYTE =VIL
Read	L	L	H	AIN								Dout	Dout	=High Z DQ15=A-1
Write	L	H	L	AIN								DIN(3)	DIN	
Reset	X	X	X	X								High Z	High Z	High Z
Temporary sector unlock	X	X	X	AIN								DIN	DIN	High Z
Output Disable	L	H	H	X								High Z	High Z	High Z
Standby	Vcc ± 0.3V	X	X	X								High Z	High Z	High Z
Sector Protect	L	H	L	SA	X	X	X	L	X	H	L	DIN	X	X
Sector Unprotected	L	H	L	X	X	X	X	H	X	H	L	DIN	X	X
Sector Protection Verify	L	L	H	SA	X	VID	X	L	X	H	L	CODE(5)	X	X

NOTES:
1. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 5.
2. VID is the Silicon-ID-Read high voltage, 11.5V to 12.5V.
3. Refer to Table 5 for valid Data-In during a write operation.
4. X can be VIL or VIH.
5. Code=00H/XX00H means unprotected.
   Code=01H/XX01H means protected.
6. A18~A12=Sector address for sector protect.
7. The sector protect and chip unprotected functions may also be implemented via programming equipment.

2. WRITE COMMANDS/COMMAND SEQUENCES

To program data to the device or erase sectors of memory, the system must drive WE and CE to VIL, and OE to VIH. The device features an Unlock Bypass mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a byte, instead of four. The "byte Program Command Sequence" section has details on programming data to the device using both standard and Unlock Bypass command sequences. An erase operation can erase one sector, multiple sectors, or the entire device. Table indicates the address space that each sector occupies. A "sector address" consists of the address bits required to uniquely select a sector. The "Writing specific address and data commands or sequences into the command register initiates device operations. Figure 1 defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence resets the device to reading array data. Section has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the auto select command sequence, the device enters the auto select mode. The system can then read auto select codes from the internal register (which is separate from the memory array) on Q7-Q0. Standard read cycle timings apply in this mode. Refer to the Auto select Mode and Auto select Command Sequence section for more information. ICC2 in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification table and timing diagrams for write operations.

Figure 1

Sector	Sector Size		Address range		Sector Address						
	Byte Mode	Word Mode	Byte Mode (x8)	Word Mode (x16)	A18	A17	A16	A15	A14	A13	A12
SA0	64Kbytes	32Kwords	00000h-0FFFFh	00000h-07FFFh	0	0	0	0	X	X	X
SA1	64Kbytes	32Kwords	10000h-1FFFFh	08000h-0FFFFh	0	0	0	1	X	X	X
SA2	64Kbytes	32Kwords	20000h-2FFFFh	10000h-17FFFh	0	0	1	0	X	X	X
SA3	64Kbytes	32Kwords	30000h-3FFFFh	18000h-1FFFFh	0	0	1	1	X	X	X
SA4	64Kbytes	32Kwords	40000h-4FFFFh	20000h-27FFFh	0	1	0	0	X	X	X
SA5	64Kbytes	32Kwords	50000h-5FFFFh	28000h-2FFFFh	0	1	0	1	X	X	X
SA6	64Kbytes	32Kwords	60000h-6FFFFh	30000h-37FFFh	0	1	1	0	X	X	X
SA7	64Kbytes	32Kwords	70000h-7FFFFh	38000h-3FFFFh	0	1	1	1	X	X	X
SA8	64Kbytes	32Kwords	80000h-8FFFFh	40000h-47FFFh	1	0	0	0	X	X	X
SA9	64Kbytes	32Kwords	90000h-9FFFFh	48000h-4FFFFh	1	0	0	1	X	X	X
SA10	64Kbytes	32Kwords	A0000h-AFFFFh	50000h-57FFFh	1	0	1	0	X	X	X
SA11	64Kbytes	32Kwords	B0000h-BFFFFh	58000h-5FFFFh	1	0	1	1	X	X	X
SA12	64Kbytes	32Kwords	C0000h-CFFFFh	60000h-67FFFh	1	1	0	0	X	X	X
SA13	64Kbytes	32Kwords	D0000h-DFFFFh	68000h-6FFFFh	1	1	0	1	X	X	X
SA14	64Kbytes	32Kwords	E0000h-EFFFFh	70000h-77FFFh	1	1	1	0	X	X	X
SA15	32Kbytes	16Kwords	F0000h-F7FFFh	78000h-7BFFFh	1	1	1	1	0	X	X
SA16	8Kbytes	4Kwords	F8000h-F9FFFh	7C000h-7CFFFh	1	1	1	1	1	0	0
SA17	8Kbytes	4Kwords	FA000h-FBFFFh	7D000h-7DFFFh	1	1	1	1	1	0	1
SA18	16Kbytes	8Kwords	FC000h-FFFFFh	7E000h-7FFFFh	1	1	1	1	1	1	X

3. READ/RESET COMMAND

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered. If program-fail or erase-fail happen, the write of F0H will reset the device to abort the operation. A valid command must then be written to place the device in the desired state.

4. READING ARRAY DATA

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Automatic Program or Automatic Erase algorithm. After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See Erase Suspend/Erase Resume Commands" for more information on this mode. The system must issue the reset command to re-enable the device for reading array data if Q5 goes high, or while in the auto select mode. See the "Reset Command" section, next.

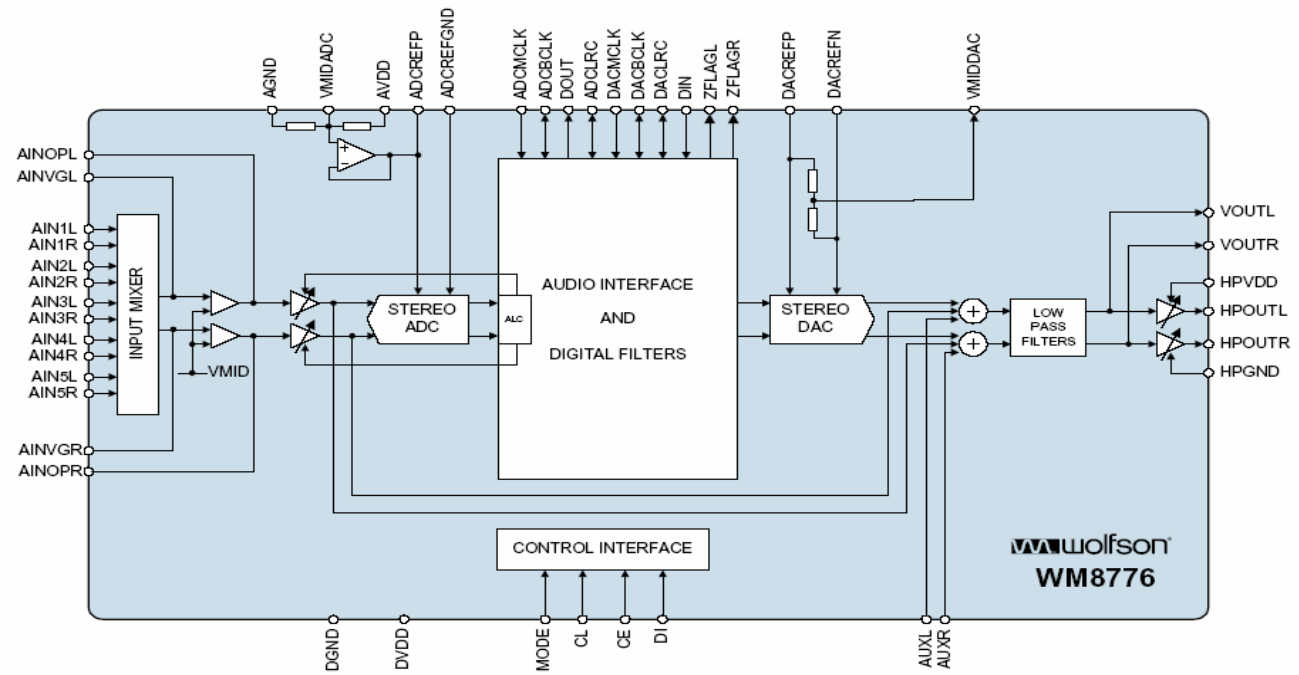
5. RESET COMMAND

Writing the reset command to the device resets the device to reading array data. Addresses bits are don't care for this command. The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete. The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete. The reset command may be written between the sequence cycles in an SILICON ID READ command sequence. Once in the SILICON ID READ mode, the reset command must be written to return to reading array data (also applies to SILICON ID READ during Erase Suspend). If Q5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

WM8776 Application

The WM8776 is a high performance, stereo audio codec with five channel input selector. The WM8776 is ideal for surround sound processing applications for home hi-fi, DVD-RW and other audiovisual equipment. Etch ADC channel has programmable gain control with automatic level control. Digital audio output word lengths from 16-32 bits and sampling rates from 32kHZ to 96KHZ are supported. The DAC has an input mixer allowing an external analogue signal to be mixed with the DAC signal. There are also Headphone and line outputs, with control for the headphone
The WM8776 supports fully independent sample rates for the ADC and DAC. The audio data interface supports I2S, left justified, right justified and DSP formats.

BLOCK DIAGRAM



1. Audio sample rate

The master clock forWM8776 supports DAC and ADC audio sampling rates 256fs to 768fs, where fs is the audio sample frequency (DACLRC or ADCLRC) typically 32KHZ, 44.1KHZ, 48KHZ or 96KHZ (the DAC also supports operation at 128fs and 192fs and 192KHZ sample rate). The master clock is used to operate the digital filters and the noise shaping circuits.

In slave mode the WM8776 has a master detection circuit that automatically determines the relationship between the master clock frequency and the sampling rate (to within +/- 32 system clocks) If there is a greater than 32 clocks error the interface is disabled and ADCLRC/DACLRC for optical performance, although the WM8776 is tolerant of phase variations or jitter on this clock. Table shows the typical master clock frequency inputs for the WM8776

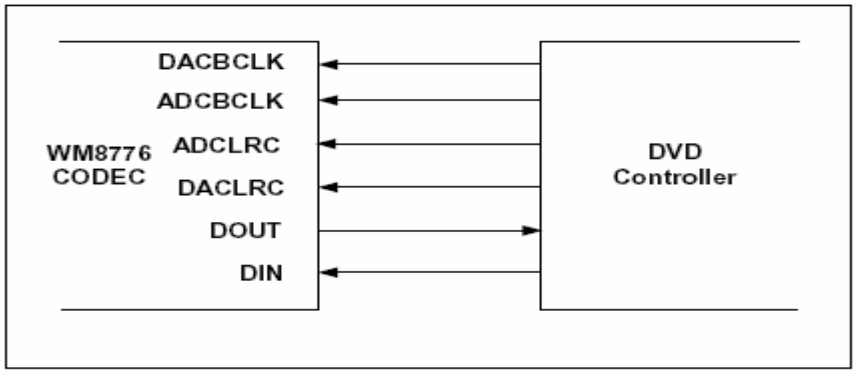
SAMPLING RATE (DACLRC/ ADCLRC)	System Clock Frequency (MHz)					
	128fs	192fs	256fs	384fs	512fs	768fs
	DAC ONLY					
32kHz	4.096	6.144	8.192	12.288	16.384	24.576
44.1kHz	5.6448	8.467	11.2896	16.9340	22.5792	33.8688
48kHz	6.144	9.216	12.288	18.432	24.576	36.864
96kHz	12.288	18.432	24.576	36.864	Unavailable	Unavailable
192kHz	24.576	36.864	Unavailable	Unavailable	Unavailable	Unavailable

2. DIGITAL AUDIO INTERFACE

1. Slave mode

The audio interfaces operations in either slave mode selectable using the MS control bit. In slave mode DIN is always an input to the WM8776 and DOUT is always an output. The default is Slave mode. In slave mode (ms=0) ADCLRC, DACLRC, ADCBCLK, DACBCLK are input to the WM8776 DIN and DACLRC are sampled by the WM8776 on the rising edge of DACBCLK; ADCLRC is sampled on the rising edge of ADCBCLK. ADC data is output on DOUT and changes on the falling edge of ADCBCLK. By setting control bit BCLKINV the polarity of ADCBCLK and DACBCLK may be reversed so that DIN and DACLRC are sample on the falling edge of DACBCLK, ADCLRC is sampled on the falling edge of ADCBCLK and DOUT changes on the rising of ADCBCLK

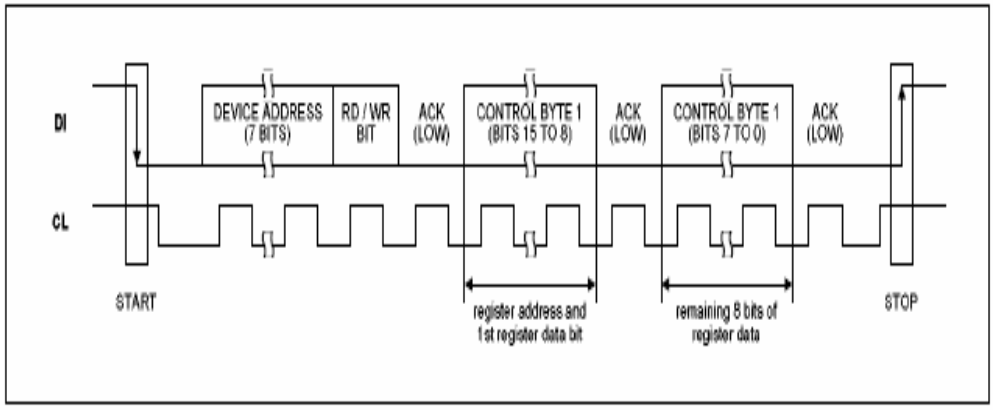
Slave mode as shown in the following figure.



2. 2 Wire serial control mode

The wm8776 supports software control via a 2-wire serial bus. Many devices can be controlled by the same bus, and each device has a unique 7-bit address (this is not the same as the 7-bit address of each register in the wm8776). The wm8776 operates as a slave device only.

2-wire serial interface as shown in the following figure.



The wm8776 has two possible device addresses, which can be selected using the CE pin
In the L32 LCD TV CE pin is LOW (device address is 34h)

CE STATE	DEVICE ADDRESS
Low	0011010 (0 x 34h)
High	0011011 (0 x 36h)

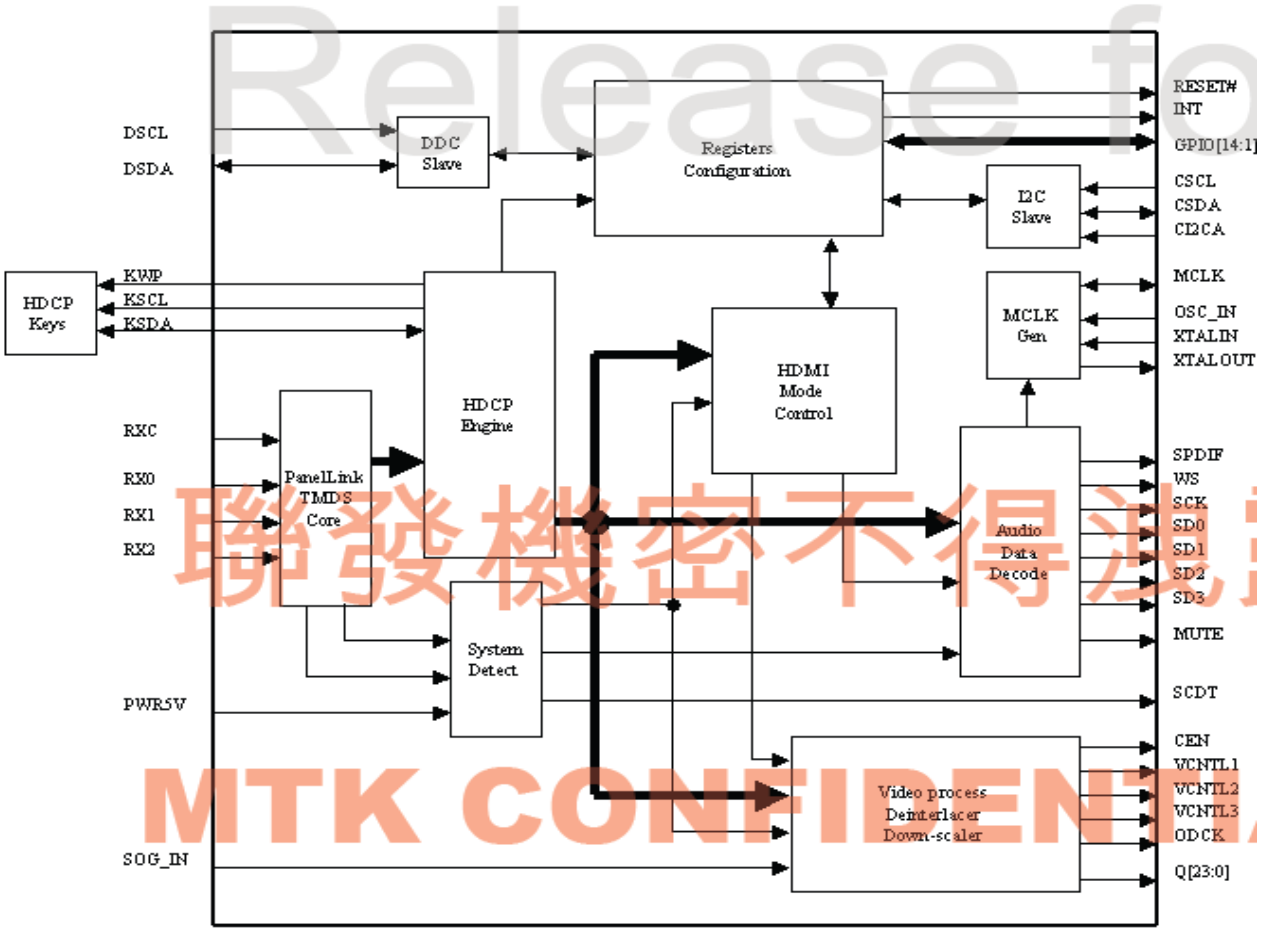
In the L32 wm8776 has 2-wire interface

MODE	Control Mode
0	2 wire interface
1	3 wire interface

MT8293 Application

The MT8293 provides a complete solution for receiving HDMI compliant digital audio and video. Specialized audio and video processing is available within the MT8293 to easily and cost effectively adds HDMI capability to consumer electronics devices such as digital TVs, plasma displays, LCD TVs and projectors.

BLOCK DIAGRAM



1. TMDS Digital Core

The core performs 10-to-8-bit TMDS decoding on the audio and video received from the three TMDS differential data lines along with a TMDS differential clock. The TMDS core supports link clock rates to 165MHZ, including CE modes to 720P/1080I/1080P.

2. Active port detection

The Pane Link core detects an active TMDS clock and actively toggling DE signal. These states are accessible in register bits, useful for monitoring the status of the HDMI input or for automatically powering down the receiver. The 5V supply from the HDMI connector is used as a cable detect indicator. The MT8293 can monitor the presence of this+5V supply and, if and when necessary, provide a fast audio mute without pops when it senses the HDMI cable pulled. The microcontroller can also poll registers in the MT8293 to check whether an HDMI cable is connected.

3. HDCP Decryption

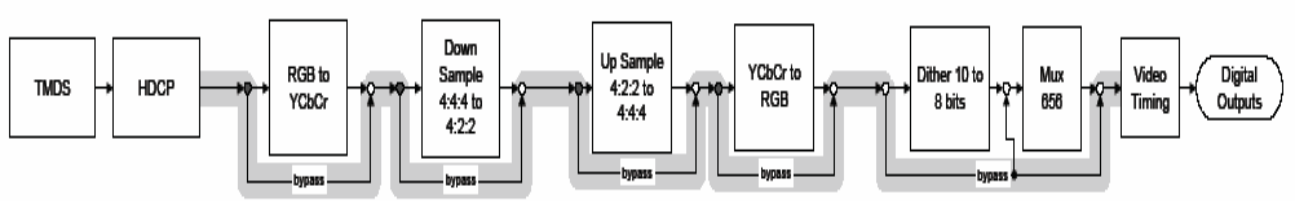
The MT8293 external EEPROM for encrypt HDCP keys. HDCP decryption contains all necessary logic to decrypt the incoming audio and video data. The decryption process is entirely controlled by the host microprocessor through a set sequence of register reads and wires through the DDC channel. Pre-programmed HDCP keys and key Selection Vector are used in the decryption process. A resulting calculated to an XOR mask during each clock cycle to decrypt the audio/video data in sync with the host.

4. Video Data Conversion and Video Output

The MT8293 can output video in many different formats as shown in the following figure.

Color Space	Video Format	Bus Width	HSYNC / VSYNC	Output Clock (MHz)[3]							Notes
				480i	480p	XGA	720p	1080i	1080p	UXGA	
RGB	4:4:4	24	Separate	13.25 / 27	27	65	74.25	74.25	148.5	162	
YCbCr	4:4:4	24	Separate	13.25 / 27	27	65	74.25	74.25	148.5	162	
YCbCr	4:2:2	16/20/24	Sep, Emb.	13.25 / 27	27	—	74.25	74.25	148.5	162	1,2
YCbCr	4:2:2	8/10/12	Sep, Emb.	27	54	135	148.5	148.5	—	—	1,4
RGB	4:4:4	48	Separate	6.73/13.5	13.5	32.25	37.13	37.13	74.25	81	5
YCbCr	4:4:4	48	Separate	6.73/13.5	13.5	32.25	37.13	37.13	74.25	81	5
RGB	4:4:4	12	Separate	13.25 / 27	27	65	74.25	74.25	—	—	6
YCbCr	4:4:4	12	Separate	13.25 / 27	27	65	74.25	74.25	—	—	6
YCbCr	4:2:2	8/10/12	Sep, Emb.	13.25/27	27	65	74.25	74.25	—	81	1,4

The receiver can also process the video data before it is output as show below figure



5. I²c Interface to Display Controller

The Controller I²c interface (CSDA, CSCL) on the MT8293 is a slave interface capable of running up to 400KHZ. This bus is used to configure the MT8293 by reading/writing to the appropriate registers. The MT8293 is accessible on the local I²c bits at two-device address. The logic state of the CI2CA pin is latched on the rising edge of REST# providing a choice of two pairs of device address.

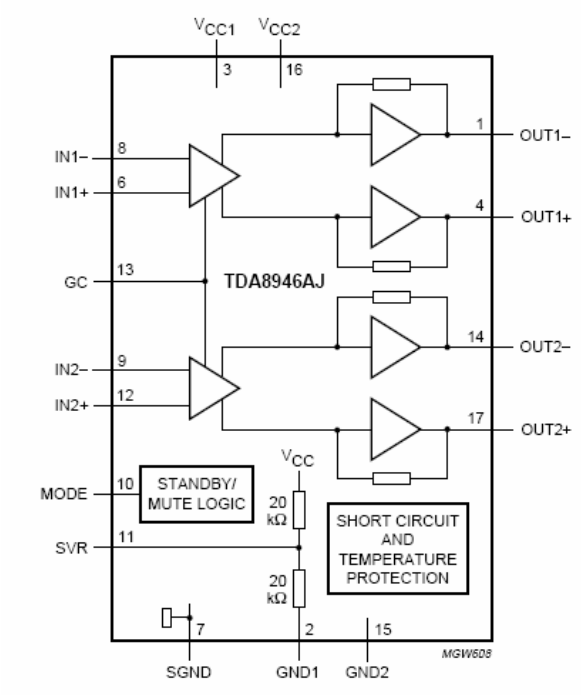
Control of local I²c address with CI2CA pin

	CI2CA = Pull Down	CI2CA = Pull Up
First Device Addr	0x60	0x62
Second Device Addr	0x68	0x6A

TDA8946 Application

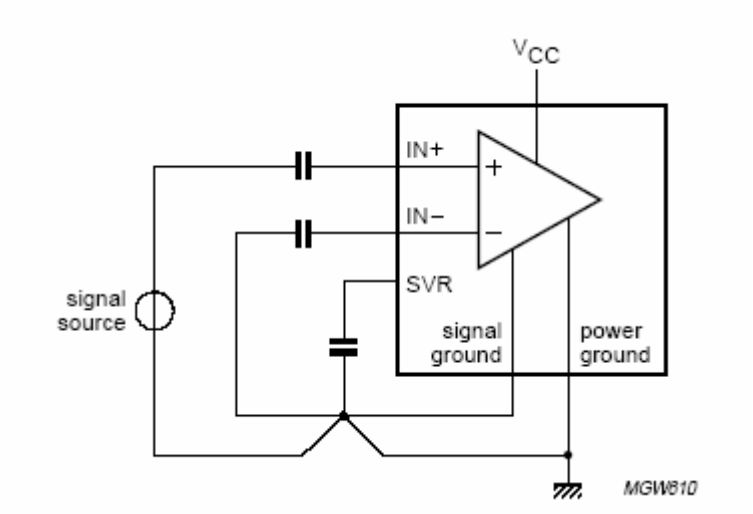
In L32 TV the TDA8946AJ is a dual-channel audio power amplifier with DC gain control. It has an output power of 2 × 10 W at an 8 Ω load and a 12 V supply.

Block diagram



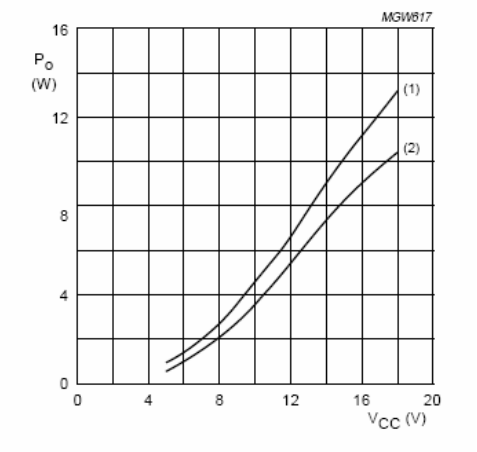
1. Input configuration

The TDA8946AJ inputs can be driven symmetrical (floating) as well as asymmetrical. In the asymmetrical mode one input pin is connected via a capacitor to the signal source and the other input is connected to the signal ground. The signal ground should be as close as possible to the SVR (electrolytic) capacitor ground. Note that the DC level of the input pins is half of the supply voltage VCC, so coupling capacitors for both pins are necessary



2. Output power measurement

The output power as a function of the supply voltage is measured on the output pins at THD = 10%,in the L32 LCD TV Vcc=12V so we can see as shown in the following figure output about 7W.



R_L = 8 Ω
(1) THD = 10%
(2) THD = 1%

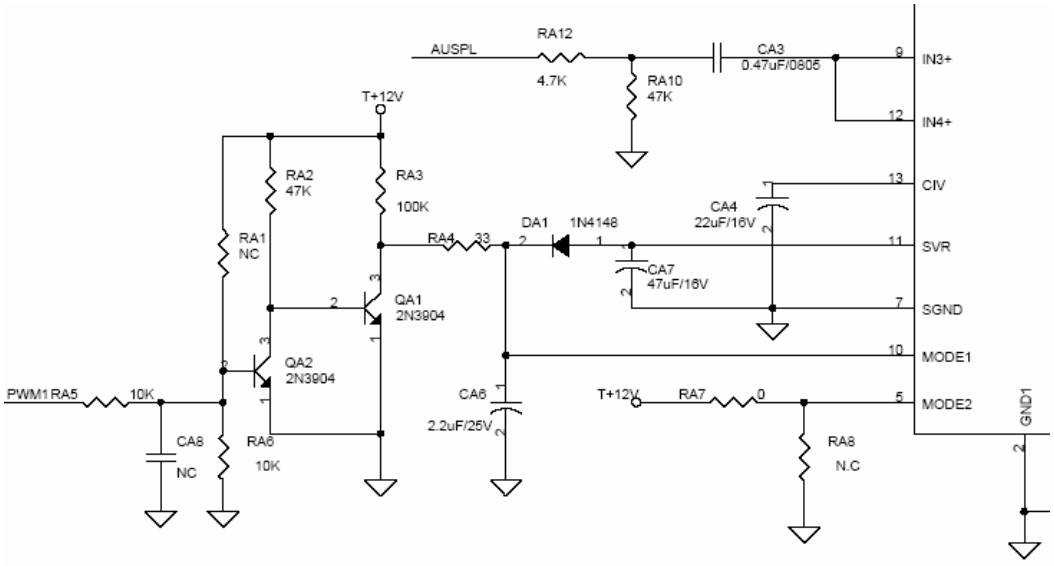
3. Mode selection

In the L32 LCD TV TDA8946AJ has two functional modes, which can be selected by applying the proper DC voltage to pin MODE.

1. Mute — In this mode the amplifier is DC-biased but not operational (no audio output).

This allows the input coupling capacitors to be charged to avoid pop-noise. The device is in mute mode when 3.5 V < VMODE < (VCC − 1.5 V).

2. Operating — In this mode the amplifier is operating normally. The operating mode is activated at VMODE<1.0V.



MT5351 Application :

MediaTek MT5351 is a DTV Backend Decoder SOC which support flexible transport demux , HD MPEG-2 video decoder , JPEG decoder , MPEG1,2,MP3,AC3 audio decoder , HDTV encoder . The MT5351 enables consumer electronics manufactures to build high quality , feature-rich DTV , STB or other home entertainment audio/video device.World-Leading Technology : HW support worldwide major broadcast network and CA standards , include ATSC , DVB , OpenCable , DirectTV , MHP.Rich Feature for high value product : To enrich the feature of DTV , the MT5351 support 1394-5C component to external DVHS . Dual display , PIP/POP and quad pictures provide user a whole new viewing experience.Credible Audio/Video Quality : The MT5351 use advanced motion-adaptive de-interlace algorithm to achieve the best movie/video playback , The embedded 4X over-sample video DAC could generate very fine display quality . Also , the audio 3D surround and equalizer provide professional entertainment.

General Feature List :

1 . Host CPU:

1. ARM 926EJ
2. 16K I-Cache and 16K D-Cache
3. 8K Data TCM and 8K instruction
4. JTAG ICE interface
5. Watch Dog timers

2 . Transport Demuxer :

1. Support 3 independent transport stream inputs
2. Support serial/parallel interface for each transport stream input
3. Support ATSC , DVB , and MPEG2 transport stream inputs.
4. Programmable sync detection.
5. Support DES/3-DES De-scramble.
6. 96 PID filter and 128 section filters.
7. Support TS recording via IEEE1394 interface.

3 . MPEG2 Decoder :

1. Support dual MPEG-2 HD decoder or up to 8 SD decoder.
2. Complaint to MP@ML , MP@HL and MPEG-1 video standards.

4 . JPEG Decoder :

1. Decode Base-line or progressive JPEG file.

5 . 2D Graphics :

1. Support multiple color modes.
2. Point , horizontal/vertical line primitive drawing.
3. Rectangle fill and gradient fill functions.
4. Bitblt with transparent , alpha blending , alpha composition and stretch.
5. Font rendering by color expansion.
6. Support clip masks.
7. YCrCb to RGB color space transfer.

6 . OSD Display :

1. 3 linking list OSDs with multiple color mode.
2. OSD scaling with arbitary ratio from 1/2x to 2x.
3. Square size , 32x32 or 64x64 pixel , hardware cursor.

7 . Video Processing :

1. Advanced Motion adaptive de-interlace on SDTV resolution.
2. Support clip
3. 3:2/2:2 pull down source detection.
4. Arbitrary ratio vertical/horizontal scaling of video , from 1/15X to 16X.
5. Support Edge preserve.
6. Support horizontal edge enhancement.
7. Support Quad-Picture.

8 . Main Display :

1. Mixing two video and three OSD and hardware cursor.
2. Contrast/Brightness adjustment.
3. Gamma correction.
4. Picture-in-Picture(PIP).
5. Picture-Out-Picture(POP).
6. 480i/576i/480p/576p/720p/1080i output

9 . Auxiliary Display :

1. Mixing one video and one OSD.
2. 480i/576i output.

10 . TV Encoder :

1. Support NTSC M/N , PAL M/N/B/D/G/H/I
2. Macrovision Rev 7.1.L1
3. CGMS/WSS.
4. Closed Captioning.
5. Six 12-bit video DACs for CVBS , S-video or RGB/YPbPr output.

11 . Digital Video Interface :

1. Support SAV/EAV.
2. Support 8/16 for SD/HD digital video input.
3. Support 8/16/24 bits digital output for main display.
4. Support 8 bits digital output for aux display.

12 . DRAM Controller :

1. Support 64Mb to 1Gb DDR DRAM devices.
2. Configurable 32/64 bit data bus interface.
3. Support DDR266 , DDR333 , DDR400 , JEDEC specification compliant SDRAM.

13 . Peripheral Bus Interface :

1. Support NOR/NAND flash.
2. Support CableCard host control bus.

14 . Audio :

1. Support Dolby Digital AC-3 decoding.
2. MPEG-1 layer I/II , MP3 decoding.
3. Dolby prologic II.
4. Main audio output : 5.1ch + 2ch (down mix)
5. Auxiliary audio output : 2ch.
6. Pink noise and white noise generator.
7. Equalizer.
8. Bass management.
9. 3D surround processing include virtual surround.
10. Audio and video lip synchronization.
11. Support reverberation.
12. SPDIF out.
13. I2S I/F.

15 . Peripherals :

1. Three UARTs with Tx and Rx FIFO , two of them have hardware flow control.
2. Two serial interfaces , one is master only the other can be set to master mode or slave mode.
3. Two PWMs.
4. IR blaster and receiver.
5. IEEE1394 link controller.
6. IDE bus : ATA/ATAPI7 UDMA mode 5 , 100MB/s.
7. Real-time clock and watchdog controller.
8. Memory card I/F : MS/MS-pro ,SD ,CF ,and MMC
9. PCMCIA/POD/CI interface

16 . IC Outline :

1. 471 Pin BGA Package.
2. 3.3V/1.2V dual Voltage.

MX29LV320BTTC (Flash) Application :

The MX29LV320AT/B is a 32-mega bit Flash memory organized as 4M bytes of 8 bits and 2M words of 16 bits. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory.

The MX29LV320AT/B is packaged in 48-pin TSOP and 48-ball CSP. It is designed to be reprogrammed and erased in system or in standard EPROM programmers. The standard MX29LV320AT/B offers access time as fast as 70ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX29LV320AT/B has separate chip enable (CE) and output enable (OE) controls.

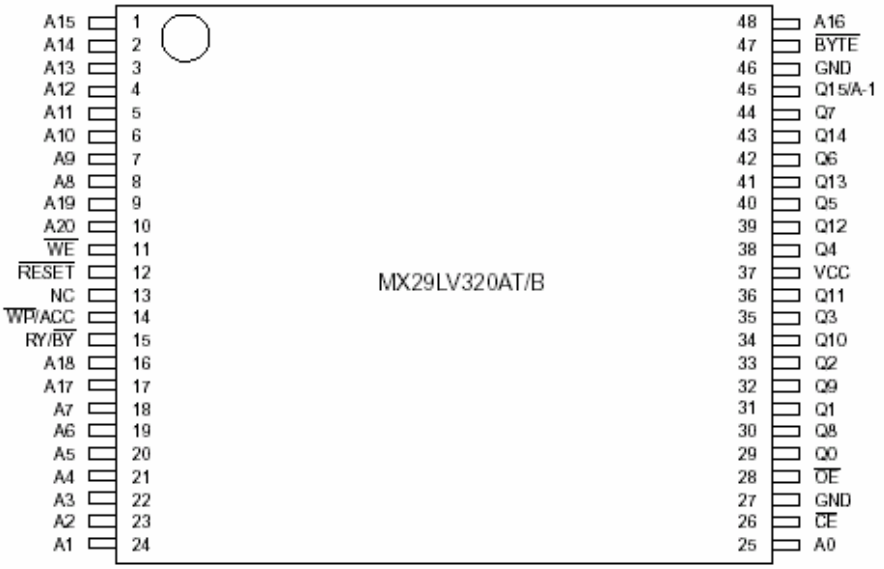
MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX29LV320AT/B uses a command register to manage this functionality. MXIC Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The MXIC cell is designed to optimize the erase and program mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling.

The MX29LV320AT/B uses a 2.7V to 3.6V VCC supply to perform the High Reliability Erase and auto Program/Erase algorithms.

The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamperes on address and data pin from -1V to VCC + 1V.

PIN CONFIGURATION

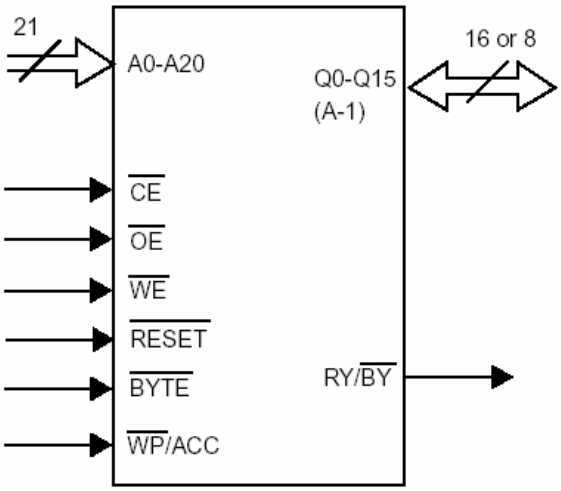
48 TSOP



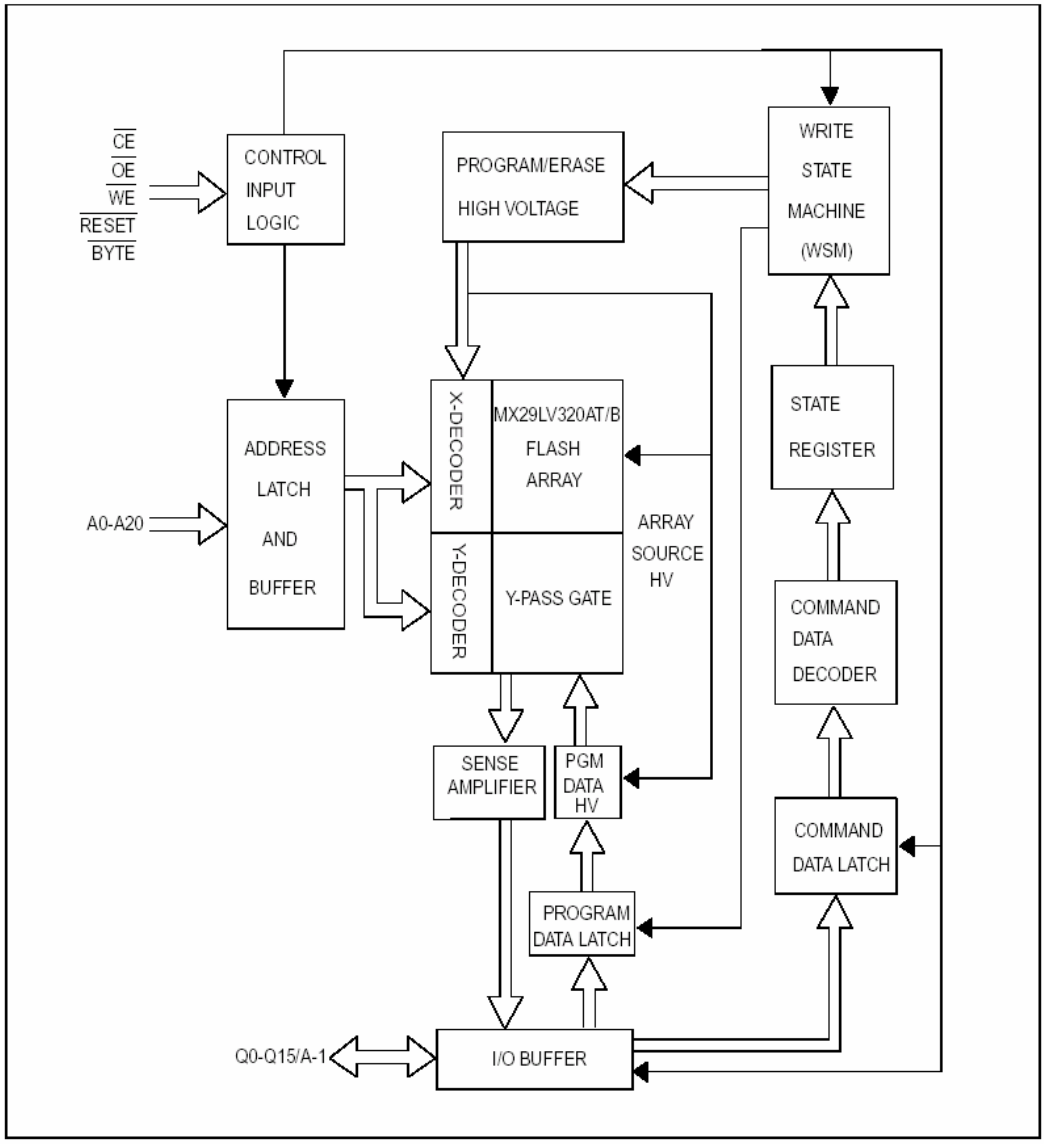
PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A20	Address Input
Q0~Q14	15 Data Inputs/Outputs
Q15/A-1	Q15(Data Input/Output, word mode) A-1(LSB Address Input, byte mode)
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{BYTE}$	Word/Byte Selection Input
$\overline{RESET}$	Hardware Reset Pin, Active Low
RY/$\overline{BY}$	Read/Busy Output
VCC	3.0 volt-only single power supply
$\overline{WP}$/ACC	Hardware Write Protect/Acceleration Pin
GND	Device Ground
NC	Pin Not Connected Internally

LOGIC SYMBOL



BLOCK DIAGRAM



BUS OPERATION--1

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	$\overline{WP}$/ACC	Addresses (Note 2)	Q0~Q7	Q8 ~ Q15	
								$\overline{Byte}$=VIH	$\overline{Byte}$=VIL
Read	L	L	H	H	L/H	A_{IN}	D_{OUT}	D_{OUT}	Q8-A14 =High-Z Q15=A-1
Write (Note 1)	L	H	L	H	Note 3	A_{IN}	D_{IN}	D_{IN}	
Accelerate Program	L	H	L	H	V_{HH}	A_{IN}	D_{IN}	D_{IN}	
Standby	VCC ± 0.3V	X	X	VCC ± 0.3V	H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	L/H	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	L/H	X	High-Z	High-Z	High-Z
Sector Group Protect (Note 2)	L	H	L	V_{ID}	L/H	Sector Addresses, A6=L, A1=H, A0=L	D_{IN}, D_{OUT}	X	X
Chip Unprotect (Note 2)	L	H	L	V_{ID}	Note 3	Sector Addresses, A6=H, A1=H, A0=L	D_{IN}, D_{OUT}	X	X
Temporary Sector Group Unprotect	X	X	X	V_{ID}	Note 3	A_{IN}	D_{IN}	D_{IN}	High-Z

Legend:

L=Logic LOW=VIL, H=Logic High=VIH, VID=12.0 0.5V, VHH=11.5-12.5V, X=Don't Care, AIN=Address IN, DIN=Data IN,DOUT=Data OUT

Notes:

1. When the WP/ACC pin is at VHH, the device enters the accelerated program mode. See "Accelerated Program Operations" for more information.

2.The sector group protect and chip unprotect functions may also be implemented via programming equipment. See the "Sector Group Protection and Chip Unprotection" section.

3.If WP/ACC=VIL, the two outermost boot sectors remain protected. If WP/ACC=VIH, the two outermost boot sector protection depends on whether they were last protected or unprotected using the method described in "Sector/Sector Block Protection and Unprotection". If WP/ACC=VHH, all sectors will be unprotected.

4.DIN or Dout as required by command sequence, data polling, or sector protection algorithm.

5.Address are A20:A0 in word mode (BYTE=VIH), A20:A-1 in byte mode (BYTE=VIL).

BUS OPERATION--2

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A20 to A12	A11 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	Q0-Q7	Q8-Q15
Read Silicon ID Manufacturer Code	L	L	H	X	X	V_{ID}	X	L	X	L	L	C2H	X
Read Silicon ID MX29LV320AT	L	L	H	X	X	V_{ID}	X	L	X	L	H	A7H	22h(word) X (byte)
Read Silicon ID MX29LV320AB	L	L	H	X	X	V_{ID}	X	L	X	L	H	A8H	22h(word) X (byte)
Sector Protect Verification	L	L	H	SA	X	V_{ID}	X	L	X	H	L	01h(1), or 00h	X
Security Sector Indicater Bit (Q7)	L	L	H	X	X	V_{ID}	X	L	X	H	H	99h(2), or 19h	X

Notes:

1.Code=00h means unprotected, or code=01h protected.

2.Code=99 means factory locked, or code=19h not factory locked.

WRITE COMMANDS/COMMAND SEQUENCES

To program data to the device or erase sectors of memory , the system must drive WE and CE to VIL, and OE to VIH.An erase operation can erase one sector, multiple sectors , or the entire device. A "sector address" consists of the address bits required to uniquely select a sector. Writing specific address and data commands or sequences into the command register initiates device operations. Table A defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence resets the device to reading array data. Section has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the Automatic Select command sequence, the device enters the Automatic Select mode. The system can then read Automatic Select codes from the internal register (which is separate from the memory array) on Q7-Q0. Standard read cycle timings apply in this mode. Refer to the Automatic Select Mode and Automatic Select Command Sequence section for more information.ICC2 in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification table and timing diagrams for write operations.

TABLE A. MX29LV320AT/B COMMAND DEFINITIONS

Command		Bus Cycles	First Bus Cycle		Second Bus Cycle		Third Bus Cycle		Fourth Bus Cycle		Fifth Bus Cycle		Sixth Bus Cycle	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read(Note 5)		1	RA	RD										
Reset(Note 4)		1	XXX	F0										
Automatic Select(Note 5)														
Manufacturer ID	Word	4	555	AA	2AA	55	555	90	X00	C2H				
	Byte	4	AAA	AA	555	55	AAA	90	X00	C2H				
Device ID	Word	4	555	AA	2AA	55	555	90	X01	ID				
	Byte	4	AAA	AA	555	55	AAA	90	X02					
Security Sector Factory	Word	4	555	AA	2AA	55	555	90	X03	99/19				
Protect Verify (Note 6)	Byte	4	AAA	AA	555	55	AAA	90	X06					
Sector Protect Verify	Word	4	555	AA	2AA	55	555	90	(SA)X02	00/01				
(Note 7)	Byte	4	AAA	AA	555	55	AAA	90	(SA)X04					
Enter Security Sector	Word	3	555	AA	2AA	55	555	88						
Region	Byte	3	AAA	AA	555	55	AAA	88						
Exit Security Sector	Word	4	555	AA	2AA	55	555	90	XXX	00				
	Byte	4	AAA	AA	555	55	AAA	90	XXX	00				
Program	Word	4	555	AA	2AA	55	555	A0	PA	PD				
	Byte	4	AAA	AA	555	55	AAA	A0	PA	PD				
Chip Erase	Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
	Byte	6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10
Sector Erase	Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
	Byte	6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	SA	30
CFI Query (Note 8)	Word	1	55	98										
	Byte	1	AA	98										
Erase Suspend(Note 9)		1	SA	B0										
Erase Resume(Note 10)		1	SA	30										

Legend:

X=Don't care
RA=Address of the memory location to be read.
RD=Data read from location RA during read operation.
PA=Address of the memory location to be programmed.
Addresses are latched on the falling edge of the WE or CE pulse.
PD=Data to be programmed at location PA. Data is latched on the rising edge of WE or CE pulse.
SA=Address of the sector to be erased or verified. Address bits A20-A12 uniquely select any sector.
ID=22A7h(Top), 22A8h(Bottom)

Notes:

1.All values are in hexadecimal.
2.Except when reading array or Automatic Select data, all bus cycles are write operation.
3.The Reset command is required to return to the read mode when the device is in the Automatic Select mode or if Q5 goes high.
4.The fourth cycle of the Automatic Select command sequence is a read cycle.
5.The data is 99h for factory locked and 19h for not factory locked.
6.The data is 00h for an unprotected sector/sector block and 01h for a protected sector/sector block. In the third cycle of the command sequence, address bit A20=0 to verify sectors 0~31, A20=1 to verify sectors 32~70 for Top Boot device.
7.Command is valid when device is ready to read array data or when device is in Automatic Select mode.
8.The system may read and program functions in non-erasing sectors, or enter the Automatic Select mode, when in the erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.
9.The Erase Resume command is valid only during the Erase Suspend mode.

STANDBY MODE

MX29LV320AT/B can be set into Standby mode with two different approaches. One is using both CE and RESET pins and the other one is using RESET pin only.

When using both pins of CE and RESET, a CMOS Standby mode is achieved with both pins held at Vcc ±0.3V. Under this condition, the current consumed is less than 0.2uA (typ.). If both of the CE and RESET are held at VIH, but not within the range of VCC ± 0.3V, the device will still be in the standby mode, but the standby current will be larger. During Auto Algorithm operation, Vcc active current (ICC2) is required even CE = "H" until the operation is completed. The device can be read with standard access time (tCE) from either of these standby modes.

When using only RESET, a CMOS standby mode is achieved with RESET input held at Vss ± 0.3V, Under this condition the current is consumed less than 1uA (typ.). Once the RESET pin is taken high, the device is back to active without recovery delay.In the standby mode the outputs are in the high impedance state, independent of the OE input.MX29LV320AT/B is capable to provide the Automatic Standby Mode to restrain power consumption during readout of data. This mode can be used effectively with an application requested low power consumption such as handy terminals.

To active this mode, MX29LV320AT/B automatically switch themselves to low power mode when MX29LV320AT/B addresses remain stable during access time of tACC+30ns. It is not necessary to control CE, WE, and OE on the mode. Under the mode, the current consumed is typically 0.2uA (CMOS level).

RESET OPERATION

01The RESET pin provides a hardware method of resetting the device to reading array data. When the RESET pin is driven low for at least a period of tRP, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET pulse. When RESET is held at VSS 0.3V, the device draws CMOS standby current (ICC4). If RESET is held at VIL but not within VSS 0.3V, the standby current will be greater.The RESET pin may be tied to system reset circuitry. A system reset would that also reset the Flash memory, enabling the system to read the boot-up firm-ware from the Flash memory.

If RESET is asserted during a program or erase operation, the RY/BY pin remains a "0" (busy) until the internal reset operation is complete, which requires a time of tREADY (during Embedded Algorithms). The system can thus monitor RY/BY to determine whether the reset operation is complete. If RESET is asserted when a program or erase operation is not executing (RY/BY pin is "1"), the reset operation is completed within a time of tREADY (not during Embedded Algorithms). The system can read data tRH after the RESET pin returns to VIH. Refer to the AC Characteristics tables for RESET parameters and to Figure 14 for the timing diagram.

WRITE PROTECT (WP)

The write protect function provides a hardware method to protect boot sectors without using VID.

If the system asserts VIL on the WP/ACC pin, the device disables program and erase functions in the two "outermost" 8 Kbyte boot sectors independently of whether those sectors were protected or unprotected using the method described in Sector/Sector Group Protection and Chip Unprotection". The two outermost 8 Kbyte boot sectors are the two sectors containing the lowest addresses in a bottom-boot-configured device, or the two sectors containing the highest addresses in a top-boot-configured device.

If the system asserts VIH on the WP/ACC pin, the device reverts to whether the two outermost 8K Byte boot sectors were last set to be protected or unprotected. That is, sector protection or unprotection for these two sectors depends on whether they were last protected or unprotected using the method described in "Sector/Sector Group Protection and Chip Unprotection".

Note that the WP/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

SOFTWARE COMMAND DEFINITIONS :

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. Table 3 defines the valid register command sequences. Note that the Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress. Either of the two reset command sequences will reset the device (whenapplicable).

All addresses are latched on the falling edge of WE or CE, whichever happens later. All data are latched on rising edge of WE or CE, whichever happens first.

WRITE OPERATION STATUS

The device provides several bits to determine the status of a write operation: Q2, Q3, Q5, Q6, Q7, and RY/BY.Table B and the following subsections describe the functions of these bits. Q7, RY/BY, and Q6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

Table B. Write Operation Status

	Status		Q7 Note1	Q6	Q5 Note2	Q3	Q2	RY/$\overline{BY}$
In Progress	Byte/Word Program in Auto Program Algorithm		$\overline{Q7}$	Toggle	0	N/A	No Toggle	0
	Auto Erase Algorithm		0	Toggle	0	1	Toggle	0
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	No Toggle	0	N/A	Toggle	1
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data	1
		Erase Suspend Program	$\overline{Q7}$	Toggle	0	N/A	N/A	0
Exceeded Time Limits	Byte/Word Program in Auto Program Algorithm		$\overline{Q7}$	Toggle	1	N/A	No Toggle	0
	Auto Erase Algorithm		0	Toggle	1	1	Toggle	0
	Erase Suspend Program		$\overline{Q7}$	Toggle	1	N/A	N/A	0

Notes:

1.Performing successive read operations from the erase-suspended sector will cause Q2 to toggle.
2.Performing successive read operations from any address will cause Q6 to toggle.
3.Reading the byte/word address being programmed while in the erase-suspend program mode will indicate logic "1" at the Q2 bit.
However, successive reads from the erase-suspended sector will cause Q2 to toggle.

Fig C. COMMAND WRITE OPERATION

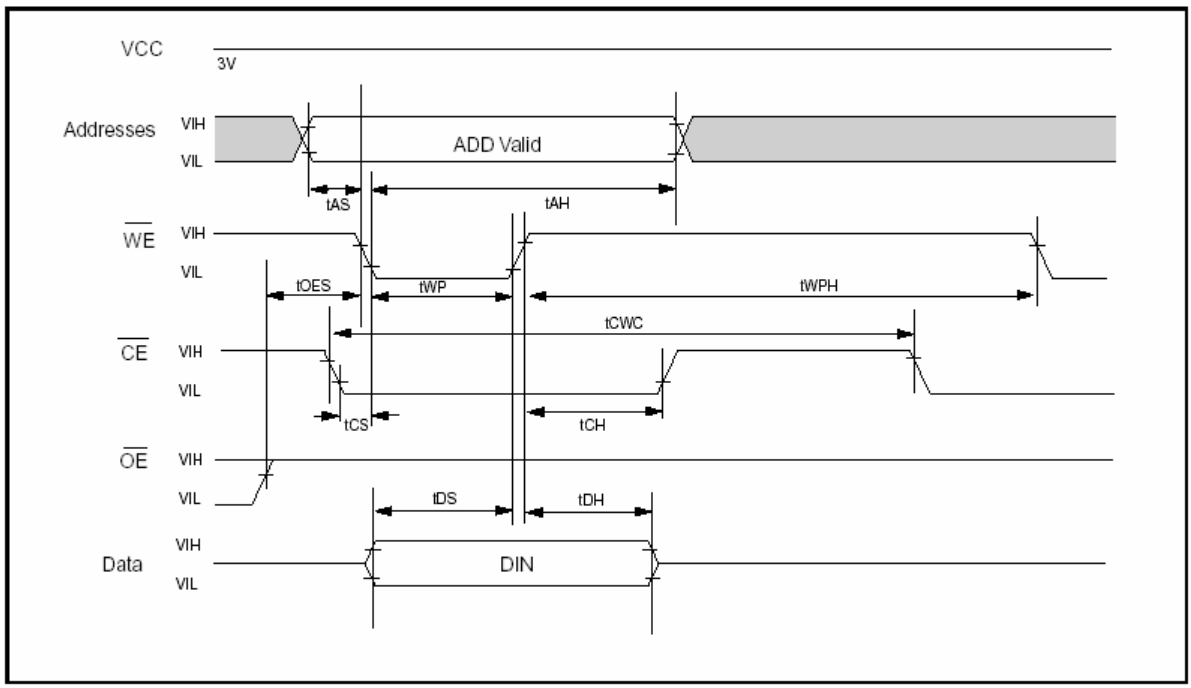
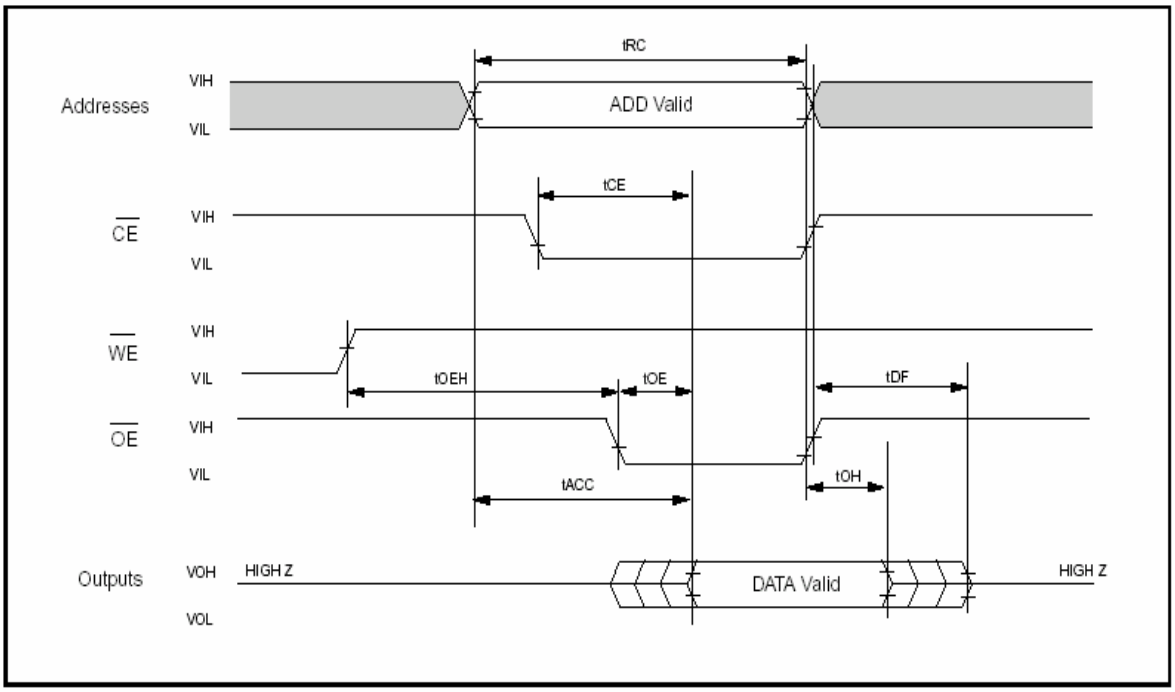


Fig D. READ TIMING WAVEFORMS

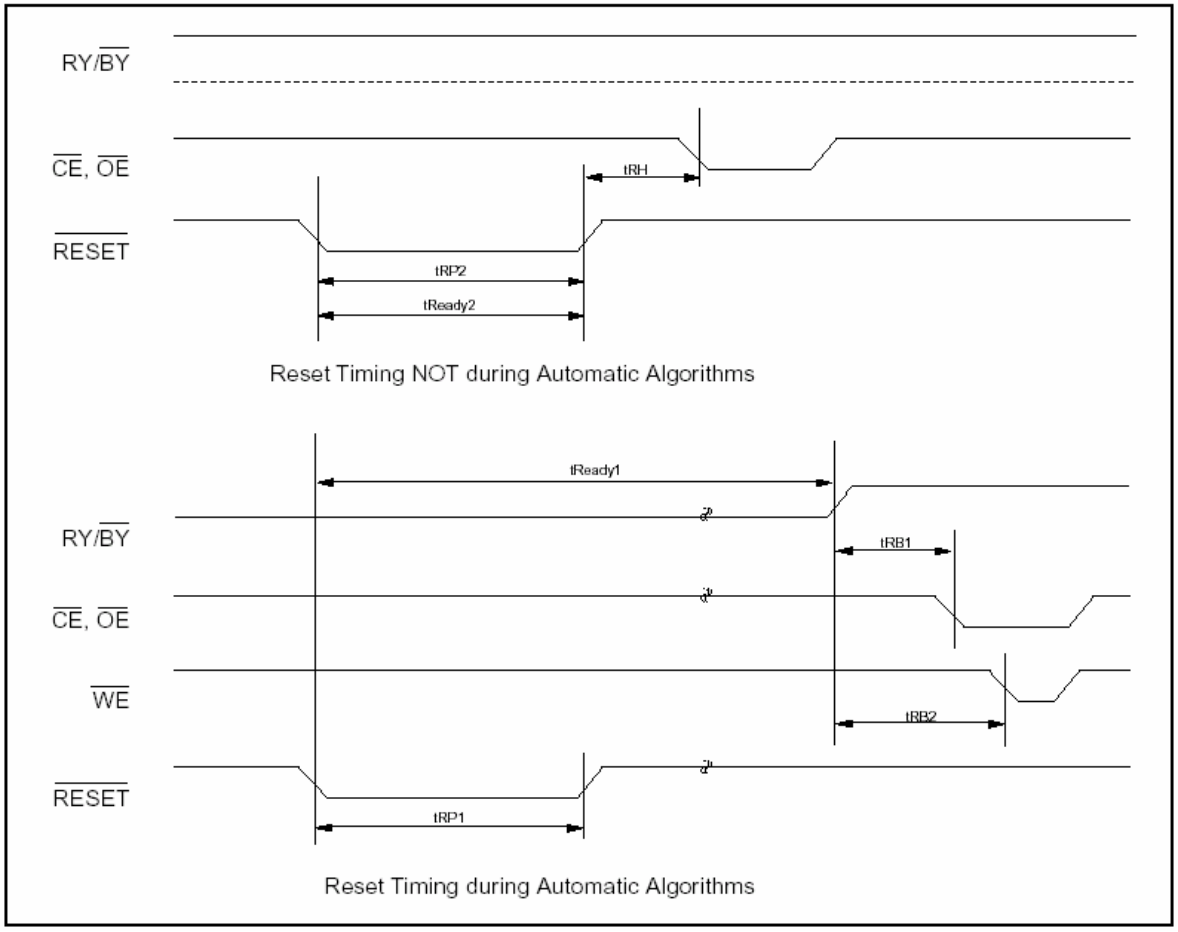


AC CHARACTERISTICS

Parameter	Description	Test Setup	All Speed Options	Unit
tREADY1	$\overline{\text{RESET}}$ PIN Low (During Automatic Algorithms) to Read or Write (See Note)	MAX	20	us
tREADY2	$\overline{\text{RESET}}$ PIN Low (NOT During Automatic Algorithms) to Read or Write (See Note)	MAX	500	ns
tRP1	$\overline{\text{RESET}}$ Pulse Width (During Automatic Algorithms)	MIN	10	us
tRP2	$\overline{\text{RESET}}$ Pulse Width (NOT During Automatic Algorithms)	MIN	500	ns
tRH	$\overline{\text{RESET}}$ High Time Before Read(See Note)	MIN	70	ns
tRB1	RY/$\overline{\text{BY}}$ Recovery Time(to $\overline{\text{CE}}$, $\overline{\text{OE}}$ go low)	MIN	0	ns
tRB2	RY/$\overline{\text{BY}}$ Recovery Time(to $\overline{\text{WE}}$ go low)	MIN	50	ns

Note:Not 100% tested

Fig E. RESET TIMING WAVEFORM

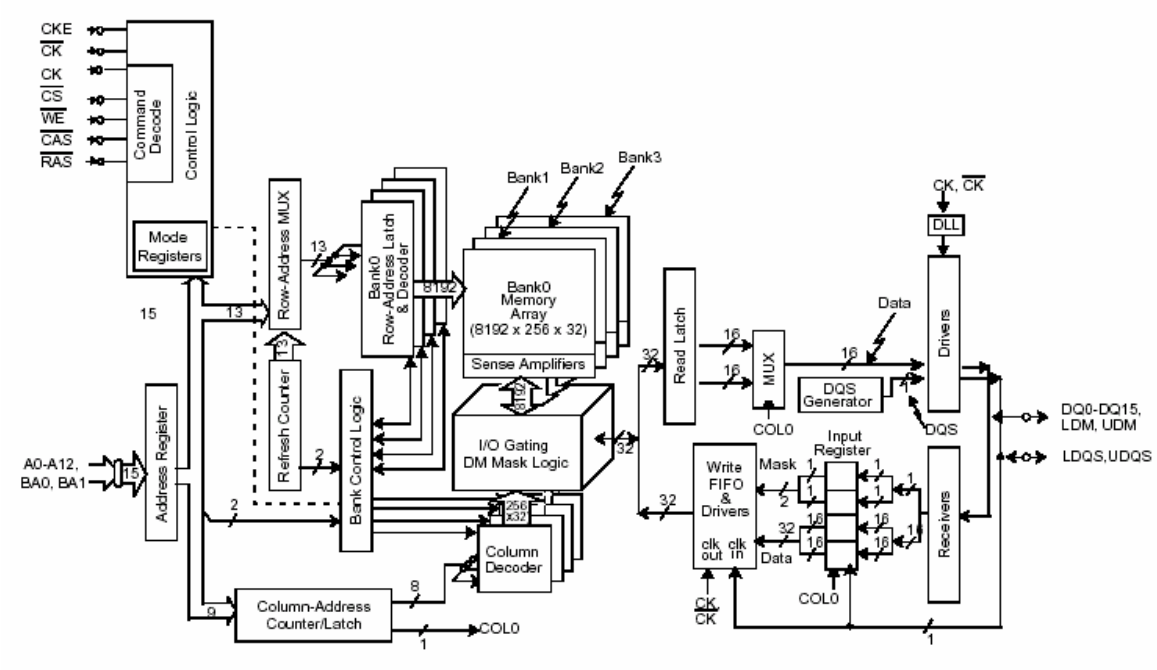


DDR SDRAM (NT5DS16M16CS-5T) Application:

Functional Description

The 256Mb DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 268, 435, 456 bits. The 256Mb DDR SDRAM is internally configured as a quad-bank DRAM. The 256Mb DDR SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double-data-rate architecture is essentially a *2n* prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 256Mb DDR SDRAM consists of a single *2n*-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins. Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A12 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access.Prior to normal operation, the DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

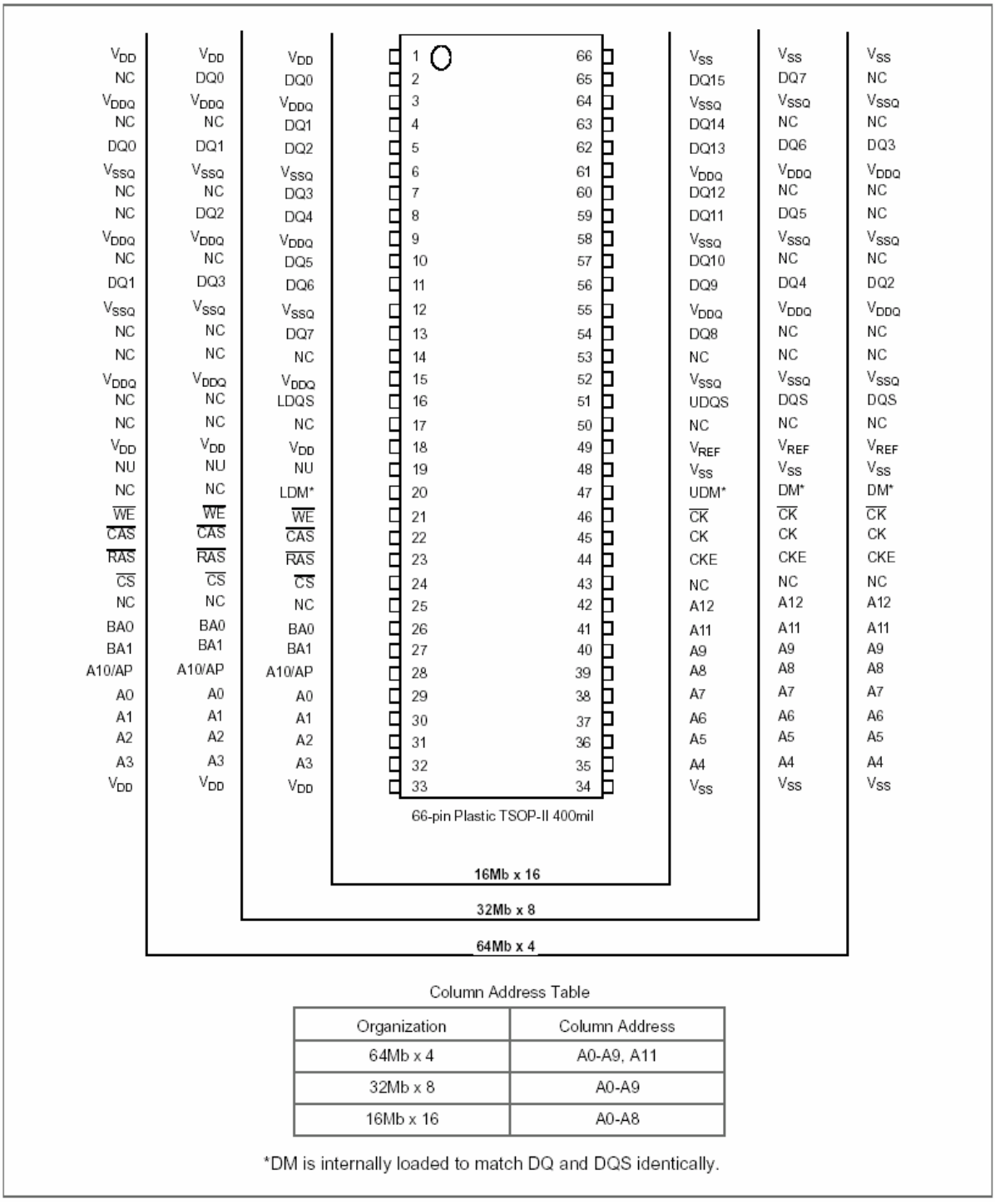
Block Diagram (16Mb x 16)



Note: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note: DM is a unidirectional signal (input only), but is internally loaded to match the load of the bidirectional DQ and DQS signals.

Pin Configuration - 400mil TSOP II (x4 / x8 / x16)

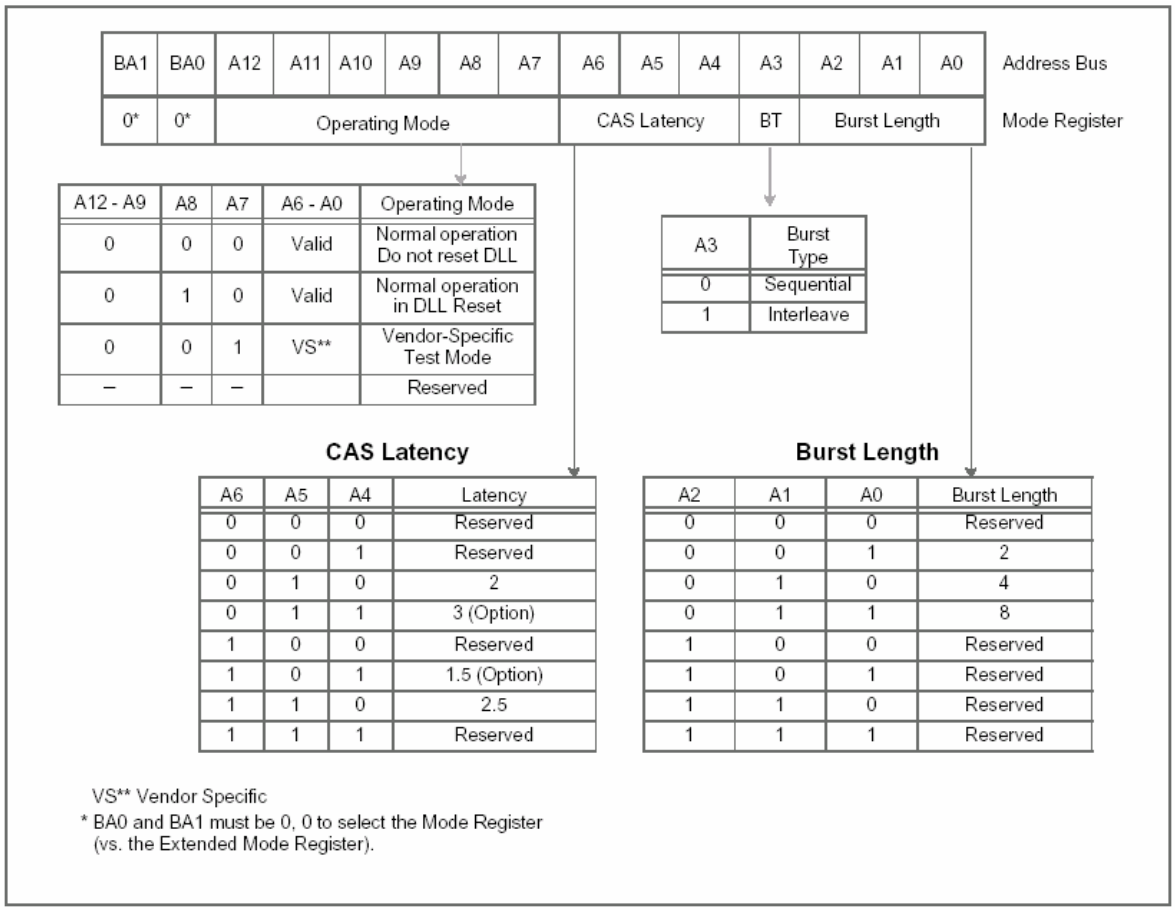


Column Address Table

Organization	Column Address
64Mb x 4	A0-A9, A11
32Mb x 8	A0-A9
16Mb x 16	A0-A8

*DM is internally loaded to match DQ and DQS identically.

Mode Register Operation



BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0*	0*	Operating Mode						CAS Latency			BT	Burst Length			Mode Register

A12 - A9	A8	A7	A6 - A0	Operating Mode
0	0	0	Valid	Normal operation Do not reset DLL
0	1	0	Valid	Normal operation in DLL Reset
0	0	1	VS**	Vendor-Specific Test Mode
–	–	–		Reserved

A3	Burst Type
0	Sequential
1	Interleave

CAS Latency

A6	A5	A4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3 (Option)
1	0	0	Reserved
1	0	1	1.5 (Option)
1	1	0	2.5
1	1	1	Reserved

Burst Length

A2	A1	A0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

VS** Vendor Specific

* BA0 and BA1 must be 0, 0 to select the Mode Register (vs. the Extended Mode Register).

Operating Mode

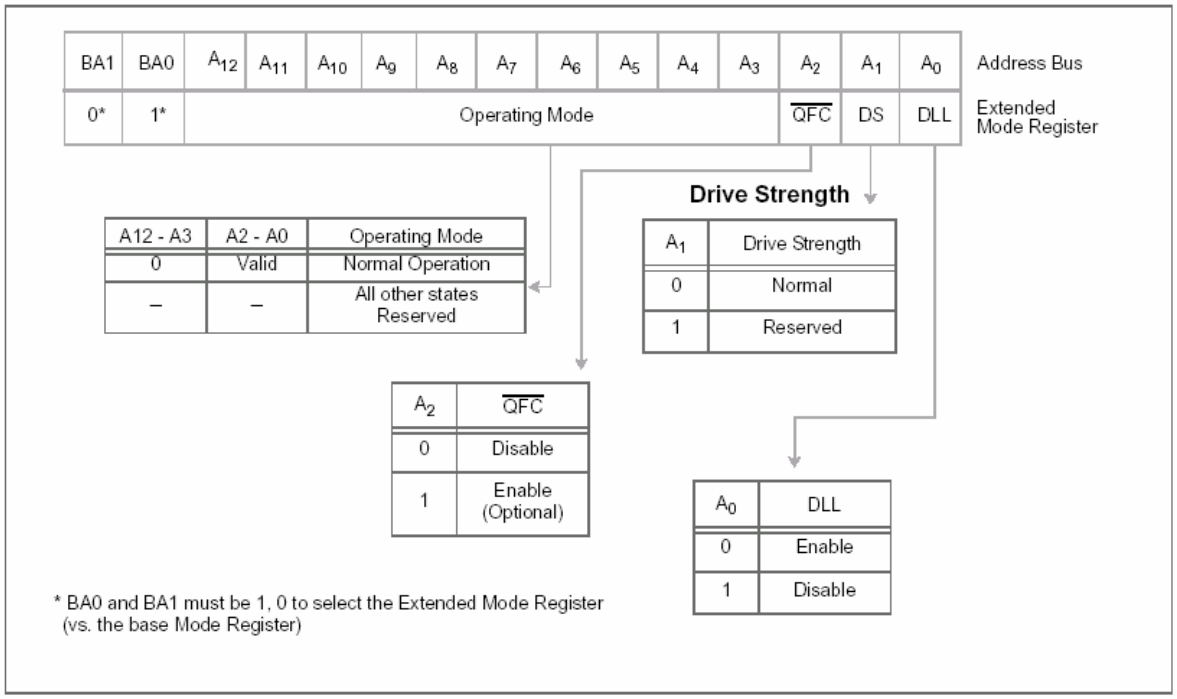
The normal operating mode is selected by issuing a Mode Register Set Command with bits A7-A12 to zero, and bits A0-A6 set to the desired values. A DLL reset is initiated by issuing a Mode Register Set command with bits A7 and A9-A12 each set to zero, bit A8 set to one, and bits A0-A6 set to the desired values. A Mode Register Set command issued to reset the DLL should always be followed by a Mode Register Set command to select normal operating mode.

All other combinations of values for A7-A12 are reserved for future use and/or test modes. Test modes and reserved states should not be used as unknown operation or incompatibility with future versions may result.

Extended Mode Register

The Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include DLL enable/disable, bit A0; output drive strength selection, bit A1; and QFC output enable/disable, bit A2 (NTC optional). These functions are controlled via the bit settings shown in the Extended Mode Register Definition. The Extended Mode Register is programmed via the Mode Register Set command (with BA0 = 1 and BA1 = 0) and retains the stored information until it is programmed again or the device loses power. The Extended Mode Register must be loaded when all banks are idle, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements result in unspecified operation.

Extended Mode Register Definition



Truth Table a: Commands

Name (Function)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	MNE	Notes
Deselect (Nop)	H	X	X	X	X	NOP	1, 9
No Operation (Nop)	L	H	H	H	X	NOP	1, 9
Active (Select Bank And Activate Row)	L	L	H	H	Bank/Row	ACT	1, 3
Read (Select Bank And Column, And Start Read Burst)	L	H	L	H	Bank/Col	Read	1, 4
Write (Select Bank And Column, And Start Write Burst)	L	H	L	L	Bank/Col	Write	1, 4
Burst Terminate	L	H	H	L	X	BST	1, 8
Precharge (Deactivate Row In Bank Or Banks)	L	L	H	L	Code	PRE	1, 5
Auto Refresh Or Self Refresh (Enter Self Refresh Mode)	L	L	L	H	X	AR / SR	1, 6, 7
Mode Register Set	L	L	L	L	Op-Code	MRS	1, 2

1. CKE is high for all commands shown except Self Refresh.
2. BA0, BA1 select either the Base or the Extended Mode Register (BA0 = 0, BA1 = 0 selects Mode Register; BA0 = 1, BA1 = 0 selects ,Extended Mode Register; other combinations of BA0-BA1 are reserved; A0-A12 provide the op-code to be written to the selected Mode Register.)
3. BA0-BA1 provide bank address and A0-A12 provide row address.
4. BA0, BA1 provide bank address; A0-A*i* provide column address (where *i* = 9 for x8 and 9, 11 for x4); A10 high enables the Auto Precharge feature (non-persistent), A10 low disables the Auto Precharge feature.
5. A10 LOW: BA0, BA1 determine which bank is precharged.A10 HIGH: all banks are precharged and BA0, BA1 are “Don’t Care.”
6. This command is auto refresh if CKE is high; Self Refresh if CKE is low.
7. Internal refresh counter controls row and bank addressing; all inputs and I/Os are “Don’t Care” except for CKE.
8. Applies only to read bursts with Auto Precharge disabled; this command is undefined (and should not be used) for read bursts with Auto Precharge enabled or for write bursts
9. Deselect and NOP are functionally interchangeable.

Active

The Active command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0,BA1 inputs selects the bank, and the address provided on inputs A0-A12 selects the row. This row remains active (or open) for accesses until a Precharge (or Read or Write with Auto Precharge) is issued to that bank. A Precharge (or Read or Write with Auto Precharge) command must be issued and completed before opening a different row in the same bank.

Read

The Read command is used to initiate a burst read access to an active (open) row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-Ai, Aj (where [i = 9, j = don't care] for x8; where [i = 9, j = 11] for x4) selects the starting column location. The value on input A10 determines whether or not Auto Precharge is used. If Auto Precharge is selected, the row being accessed is precharged at the end of the Read burst; if Auto Precharge is not selected, the row remains open for subsequent accesses.

Write

The Write command is used to initiate a burst write access to an active (open) row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-Ai, Aj (where [i = 9, j = don't care] for x8; where [i = 9, j = 11] for x4) selects the starting column location. The value on input A10 determines whether or not Auto Precharge is used. If Auto Precharge is selected, the row being accessed is precharged at the end of the Write burst; if Auto Precharge is not selected, the row remains open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered low, the corresponding data is written to memory; if the DM signal is registered high, the corresponding data inputs are ignored, and a Write is not executed to that byte/column location.

Auto Refresh

Auto Refresh is used during normal operation of the DDR SDRAM and is analogous to CAS Before RAS (CBR) Refresh in previous DRAM types. This command is nonpersistent, so it must be issued each time a refresh is required.The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an Auto Refresh command. The 256Mb DDR SDRAM requires Auto Refresh cycles at an average periodic interval of 7.8 μs (maximum).

Self Refresh

The Self Refresh command can be used to retain data in the DDR SDRAM, even if the rest of the system is powered down.When in the self refresh mode, the DDR SDRAM retains data without external clocking. The Self Refresh command is initiated as an Auto Refresh command coincident with CKE transitioning low. The DLL is automatically disabled upon entering Self Refresh, and is automatically enabled upon exiting Self Refresh (200 clock cycles must then occur before a Read command can be issued). Input signals except CKE (low) are "Don't Care" during Self Refresh operation.

The procedure for exiting self refresh requires a sequence of commands. CK (and CK) must be stable prior to CKE returning high. Once CKE is high, the SDRAM must have NOP commands issued for tXSNR because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOPs for 200 clock cycles before applying any other command.

Operations:

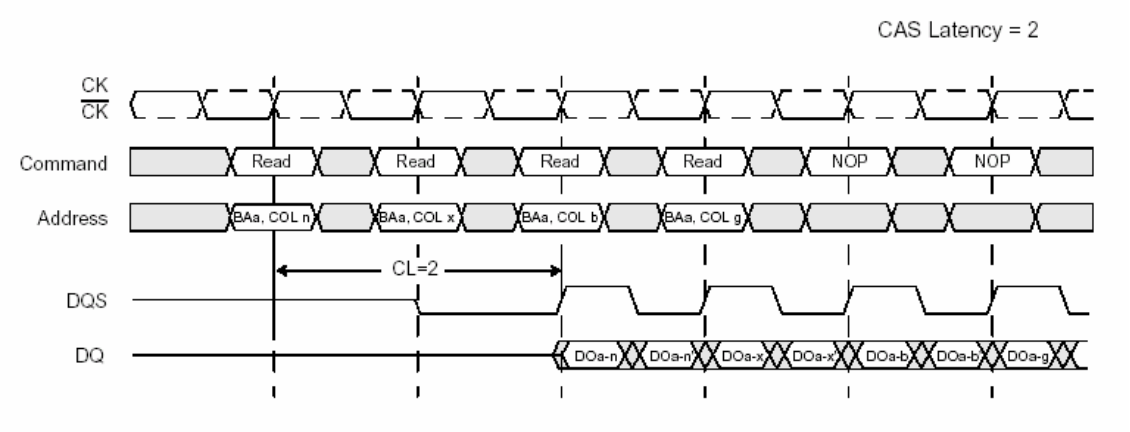
Reads

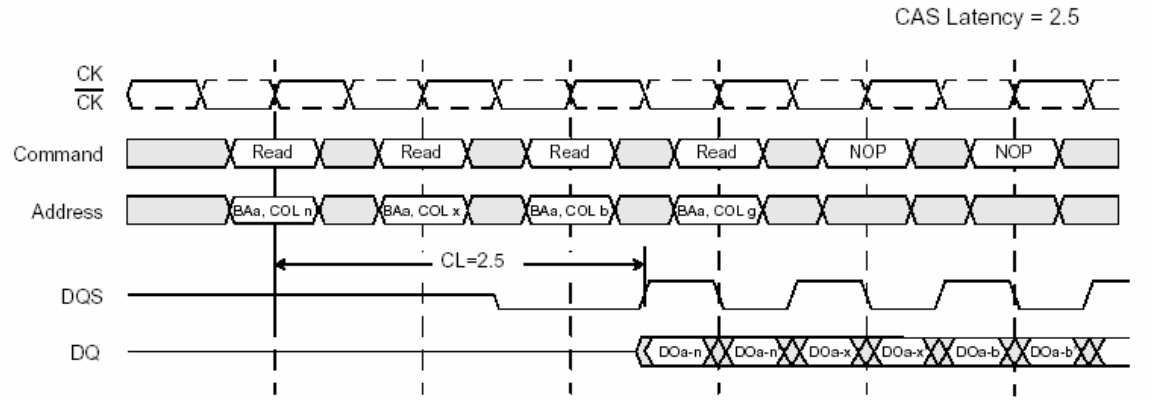
Subsequent to programming the mode register with CAS latency, burst type, and burst length, Read bursts are initiated with a Read command.

The starting column and bank addresses are provided with the Read command and Auto Precharge is either enabled or disabled for that burst access. If Auto Precharge is enabled, the row that is accessed starts precharge at the completion of the burst, provided tRAS has been satisfied. For the generic Read commands used in the following illustrations, Auto Precharge is disabled.

During Read bursts, the valid data-out element from the starting column address is available following the CAS latency after the Read command. Each subsequent data-out element is valid nominally at the next positive or negative clock edge (i.e. at the next crossing of CK and CK). The following timing figure entitled “Read Burst: CAS Latencies (Burst Length=4)” illustrates the general timing for each supported CAS latency setting. DQS is driven by the DDR SDRAM along with output data. The initial low state on DQS is known as the read preamble; the low state coincident with the last data-out element is known as the read postamble . Upon completion of a burst, assuming no other commands have been initiated, the DQs and DQS goes High-Z. Data from any Read burst may be concatenated with or truncated with data from a subsequent Read command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new Read command should be issued x cycles after the first Read command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). This is shown in timing figure entitled “Consecutive Read Bursts: CAS Latencies (Burst Length =4 or 8)”.A Read command can be initiated on any positive clock cycle following a previous Read command. Nonconsecutive Read data is shown in timing figure entitled “Non-Consecutive Read Bursts: CAS Latencies (Burst Length = 4)”. Full-speed Random Read Accesses: CAS Latencies (Burst Length = 2, 4 or 8) within a page (or pages) can be performed as shown on following:

Random Read Accesses: CAS Latencies (Burst Length = 2, 4 or 8)

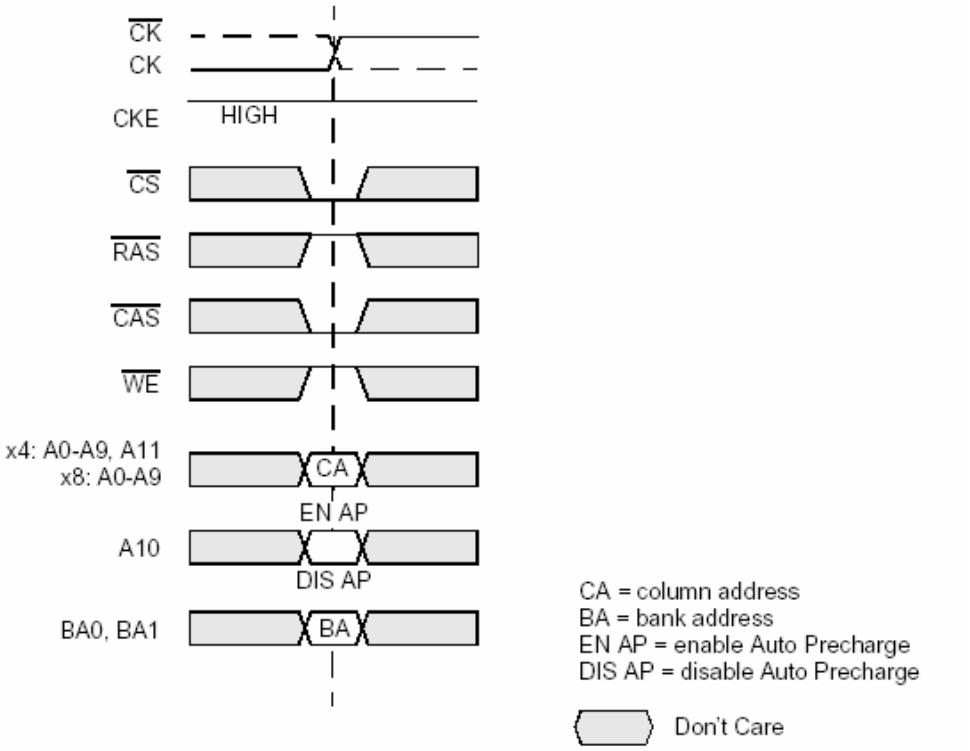




DO a-n, etc. = data out from bank a, column n etc.
n' etc. = odd or even complement of n, etc. (i.e., column address LSB inverted).
Reads are to active rows in any banks.
Shown with nominal t_{AC}, t_{DQSCK}, and t_{DQSQ}.

Don't Care

Read Command



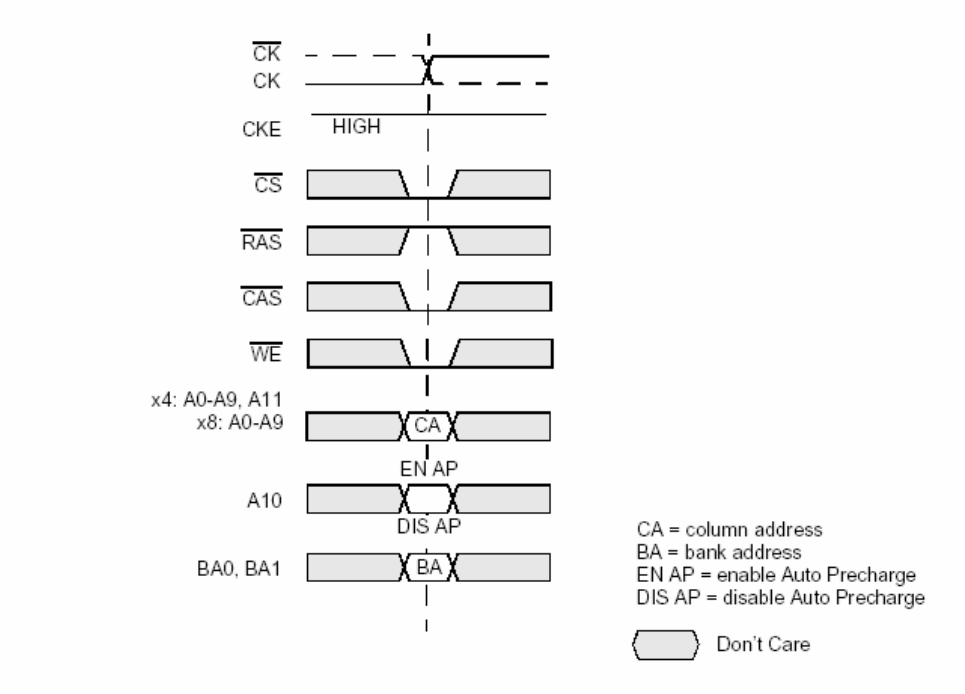
Writes

Write bursts are initiated with a Write command, as shown in timing figure *Write Command* on following: The starting column and bank addresses are provided with the Write command, and Auto Precharge is either enabled or disabled for that access. If Auto Precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic Write commands used in the following illustrations, Auto Precharge is disabled.

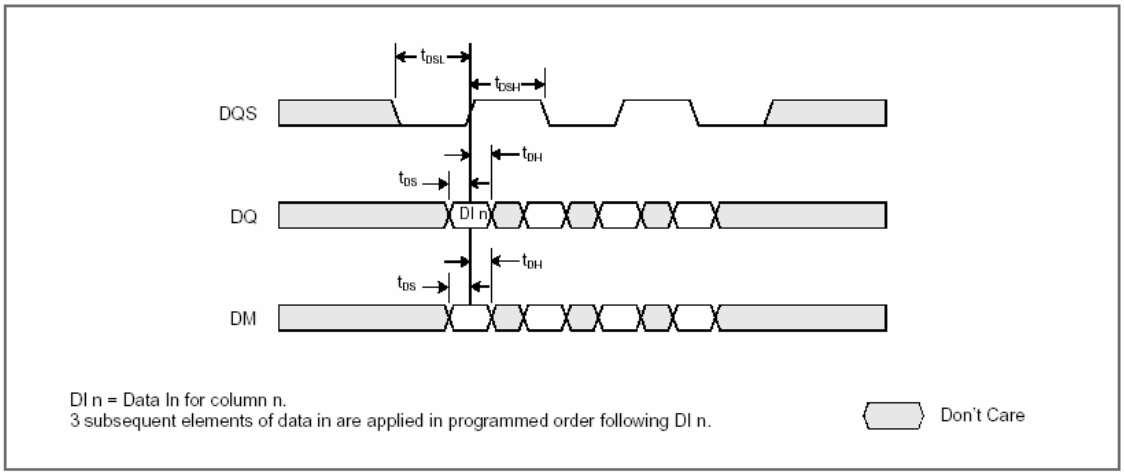
During Write bursts, the first valid data-in element is registered on the first rising edge of DQS following the write command, and subsequent data elements are registered on successive edges of DQS. The Low state on DQS between the Write command and the first rising edge is known as the write preamble; the Low state on DQS following the last data-in element is known as the write postamble.

The time between the Write command and the first corresponding rising edge of DQS (tDQSS) is specified with a relatively wide range (from 75% to 125% of one clock cycle), so most of the Write diagrams that follow are drawn for the two extreme cases (i.e. tDQSS(min) and tDQSS(max)). Timing figure *Write Burst (Burst Length = 4)* on page 33 shows the two extremes of tDQSS for a burst of four. Upon completion of a burst, assuming no other commands have been initiated, the DQs and DQS enters High-Z and any additional input data is ignored.Data for any Write burst may be concatenated with or truncated with a subsequent Write command. In either case, a continuous flow of input data can be maintained. The new Write command can be issued on any positive edge of clock following the previous Write command. The first data element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new Write command should be issued x cycles after the first Write command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture).

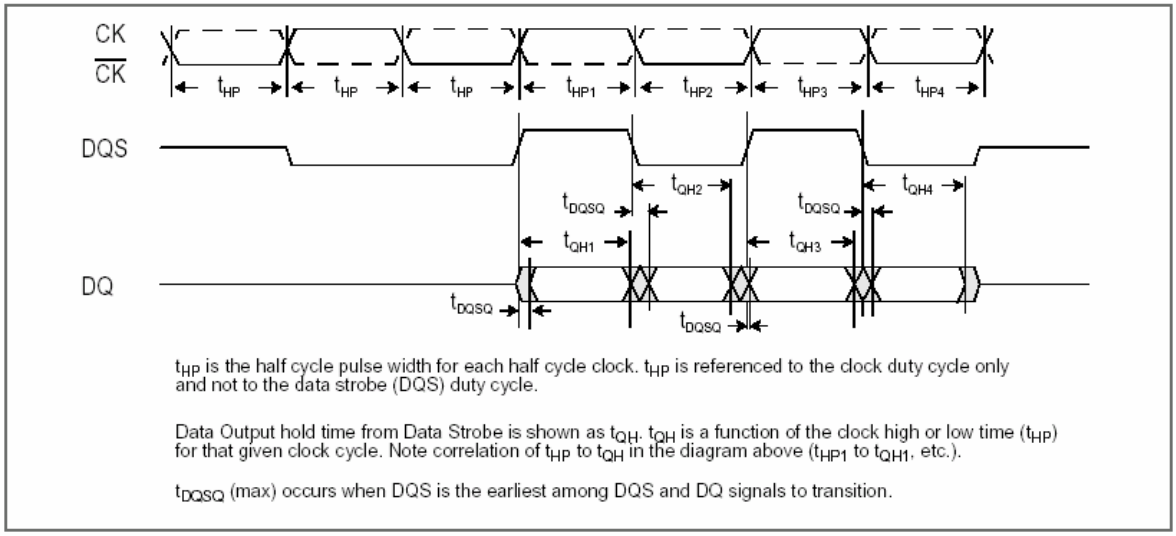
Write Command



Data Input (Write)



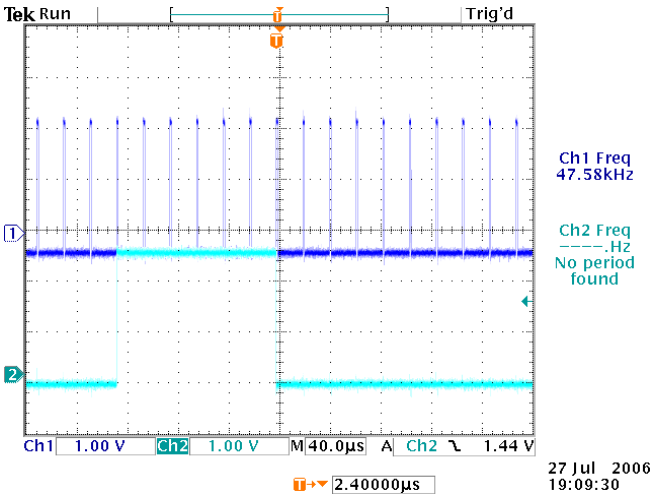
Data Output (Read)



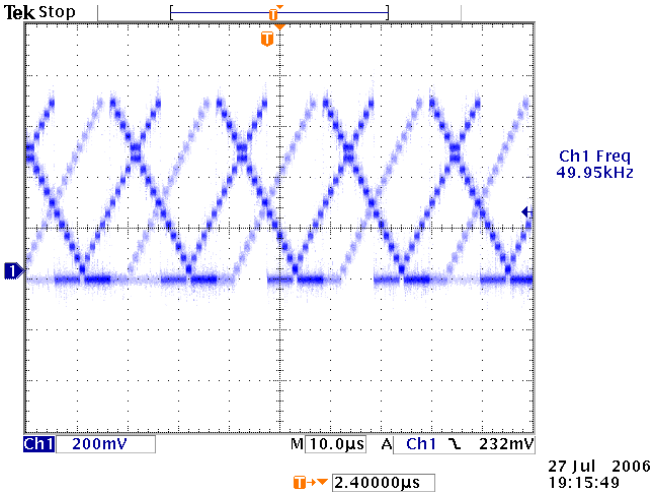
Chapter8 Waveforms

PC MODE(1366X768 60HZ)

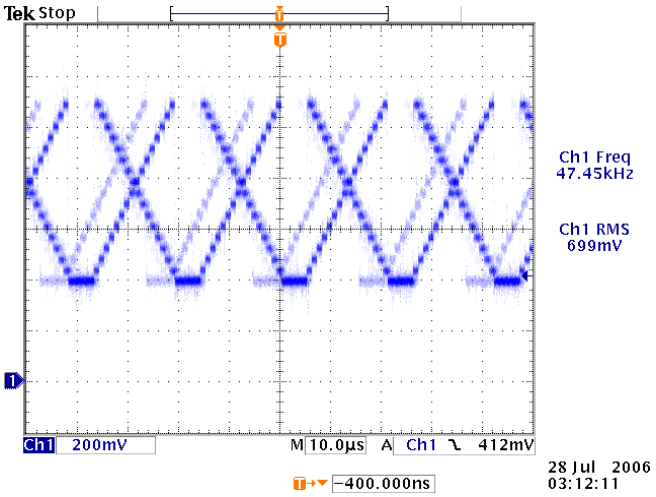
CH1 H-sync (L21); CH2 V-sync (L22)



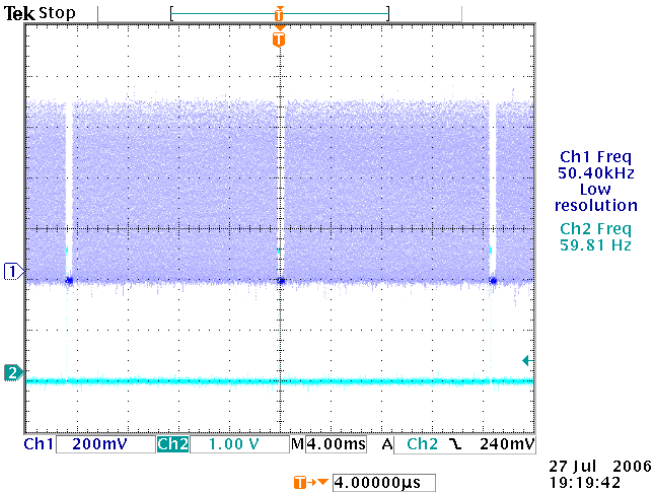
CH1 GREEN (FB27)



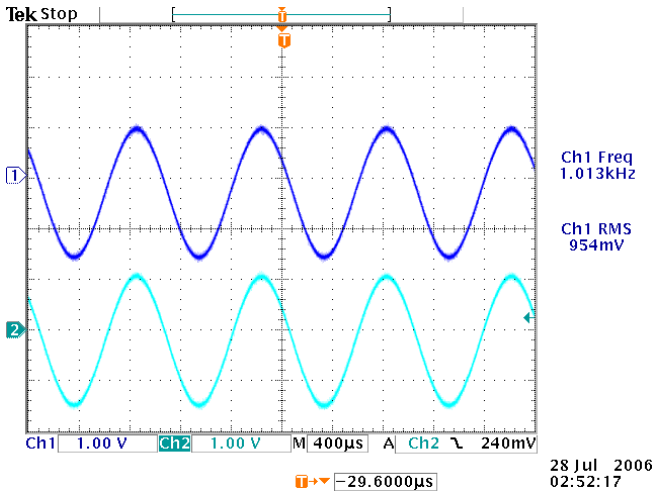
CH1 GREEN+(C294)



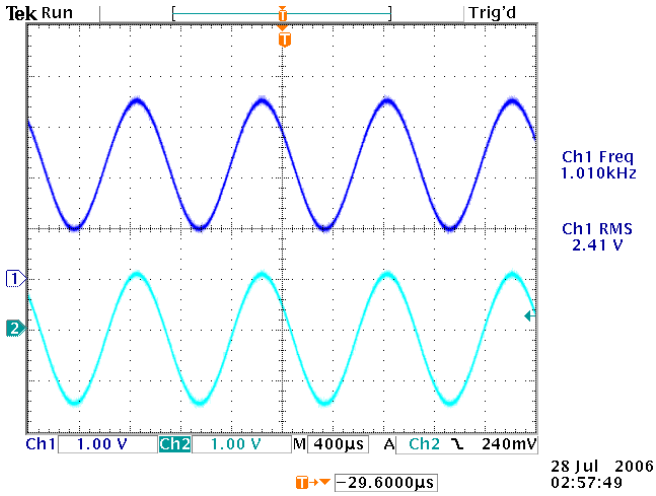
CH1 GREEN # (FB27); CH2 VGAVSYNC (L22)



CH1 VGAL (R193); CH2 AVOL (R194)

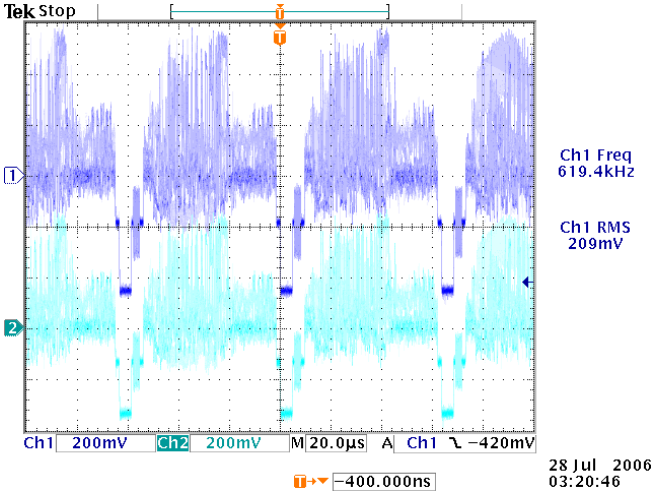


CH1 PC_L (CE70+) ; PC_L (CE70-)

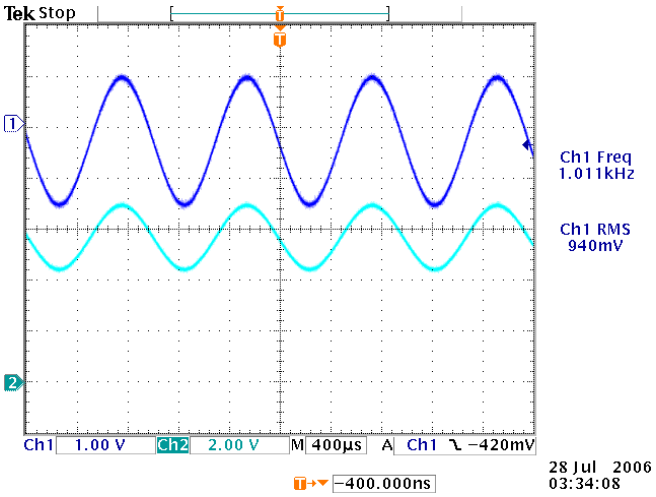


AV&TV MODE (AV1/AV2/TV) VIDEO

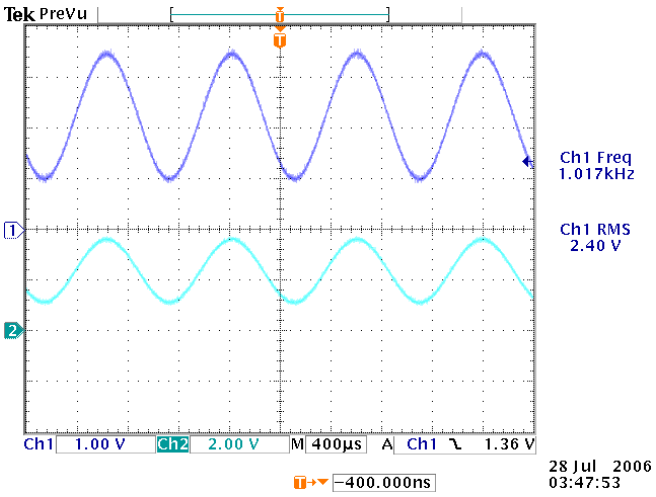
CH1 CVBS2 (R169); CH2 AV2CVBS (C255)



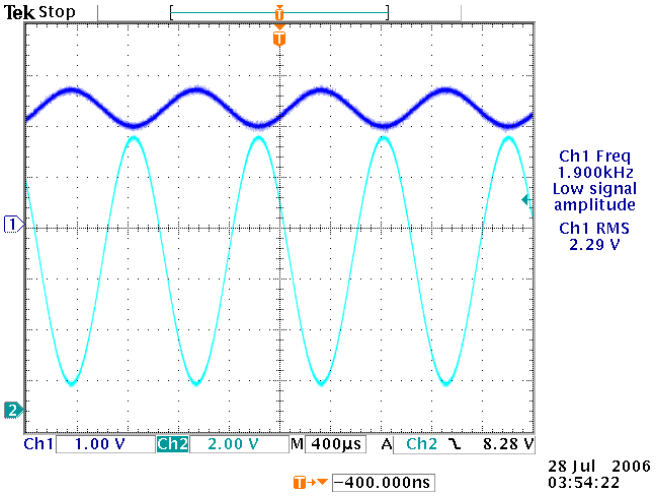
CH1 AV2L (R237); CH2 AV2L (U22 PIN14)



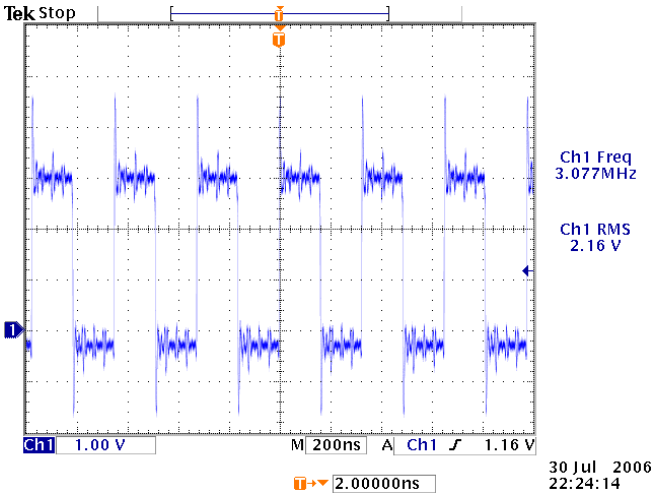
CH1 AV_L (U22 PIN13) ; CH2 AV_L (CE71-)



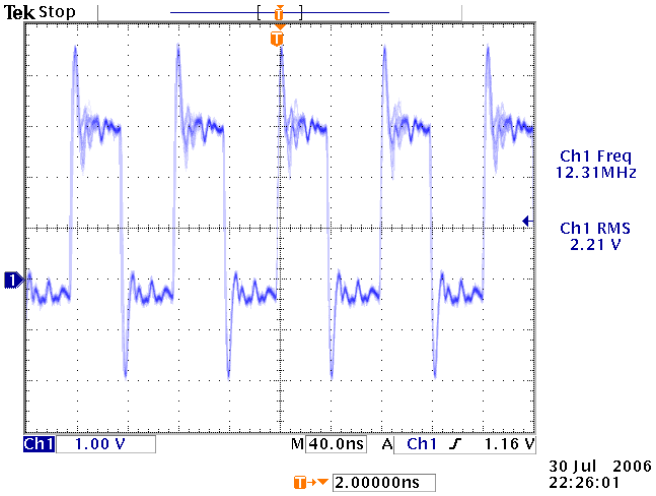
CH1 AUSPL (R302);CH2 OUT2+5(J4 PIN4)



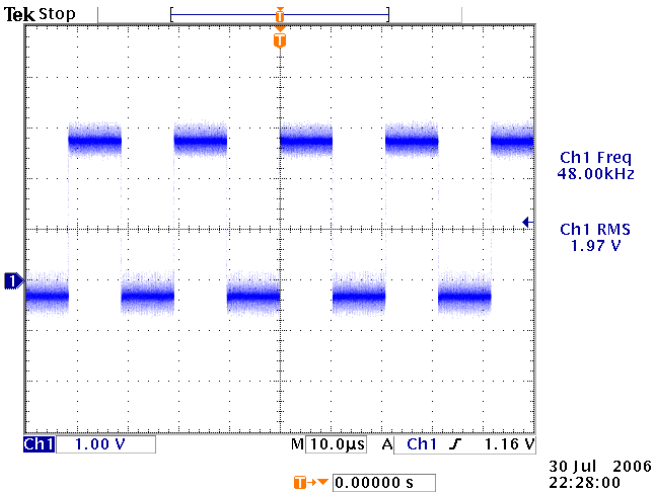
CH1 DACBCLK (U23 PIN4);



CH1 DACMCLK (U23 PIN5);

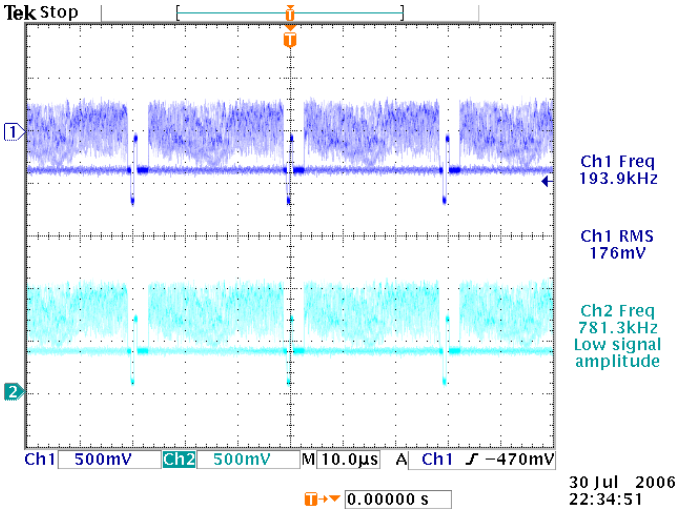


CH1 DACLRCK (U23 PIN7)

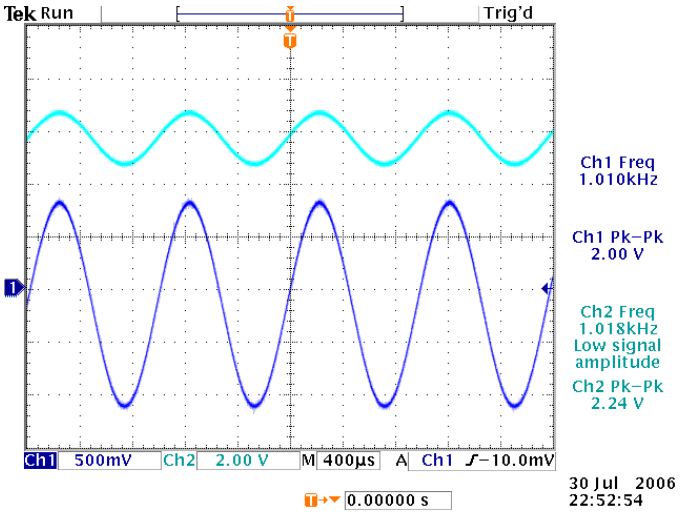


COMPONENT MODE (COMPONENT 1/2)

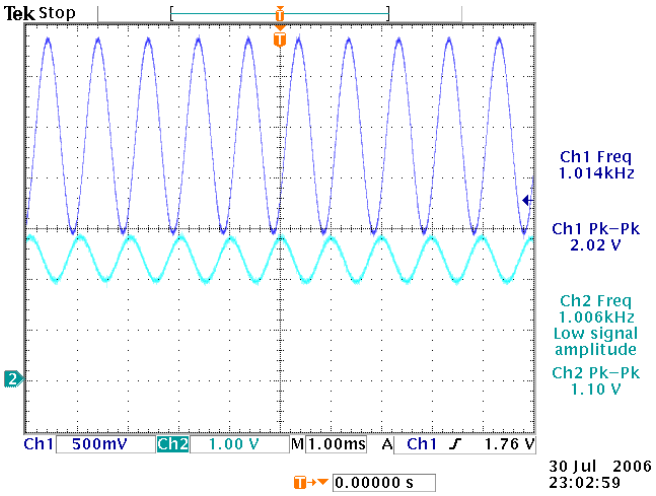
CH1 COM_Y2 (L16); CH2 AVY1P (C269)



CH1YCBCR_L2(L19) CH2 2A33 (U22 PIN11)

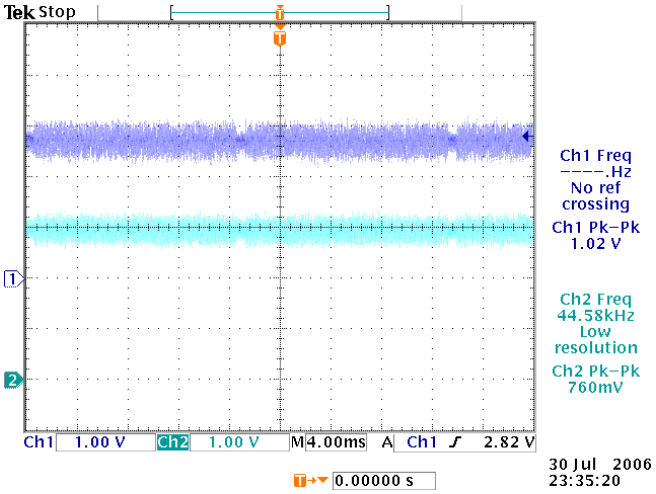


CH1 AV_L (CE71+);CH2 AUSPL (R304)

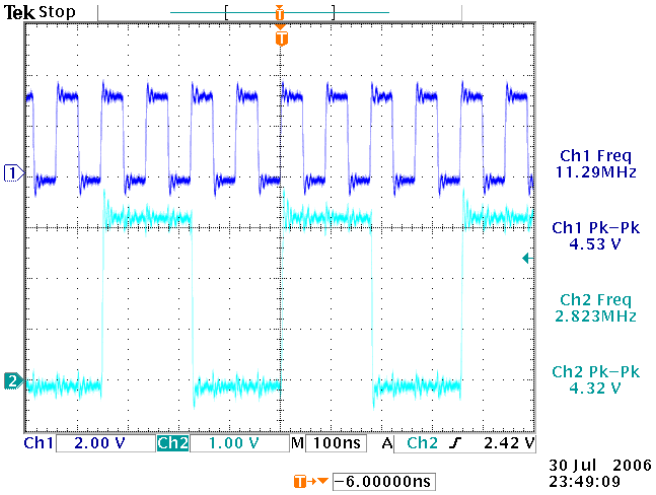


HDMI 1&2

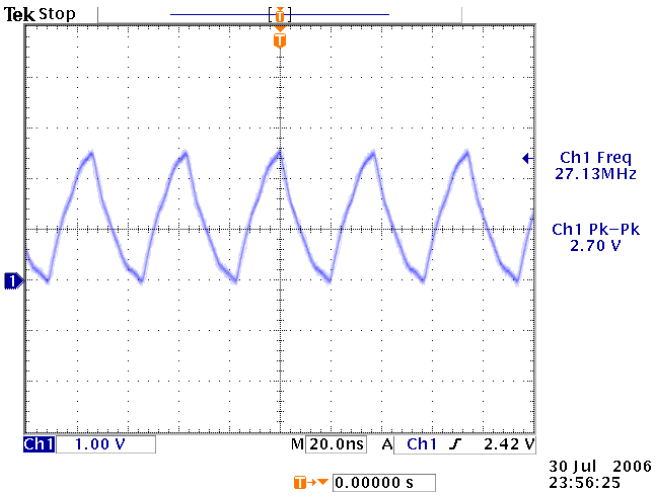
CH1 RX1_2 (P11 PIN 1); CH2 DATA2+ (U31 PIN3)



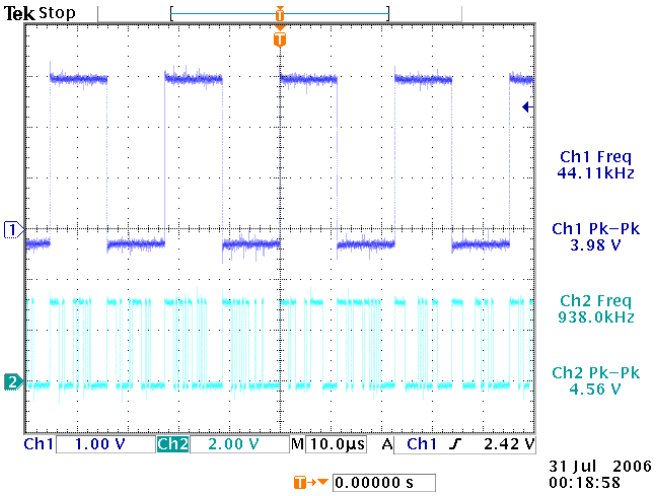
CH1 HDMIMCLK (U19 PIN 79) ;CH2 HDMIBCLK (U19 PIN 76)



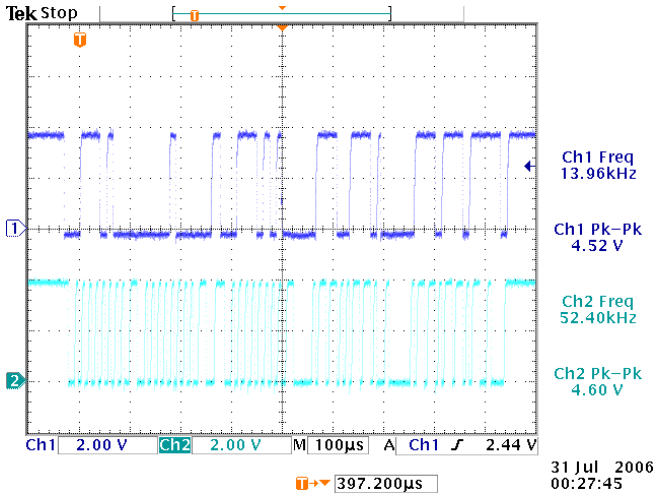
CH1 SOG_IN (U19 PIN4)



CH1 HDMILRCK (U19 PIN75) CH2 HDMISDO (U19 PIN74)

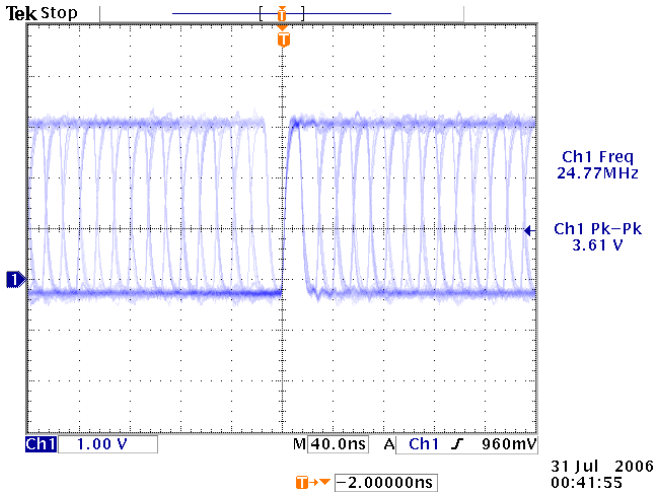


CH1 DDC_SDA (Q14 PIN3);CH2 DDC_SCL (Q13 PIN3)

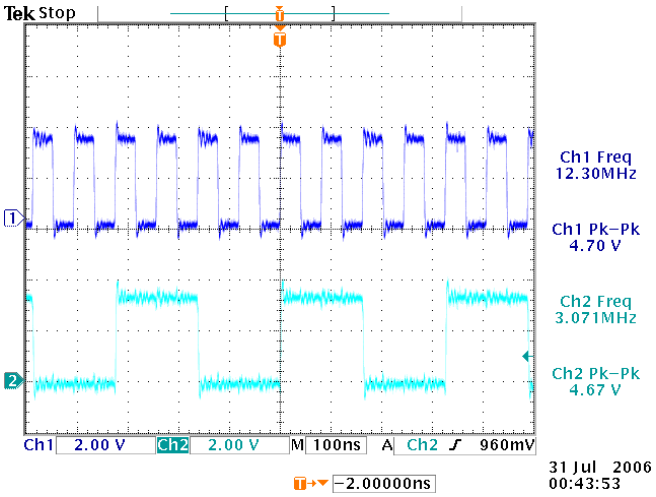


DTV HD

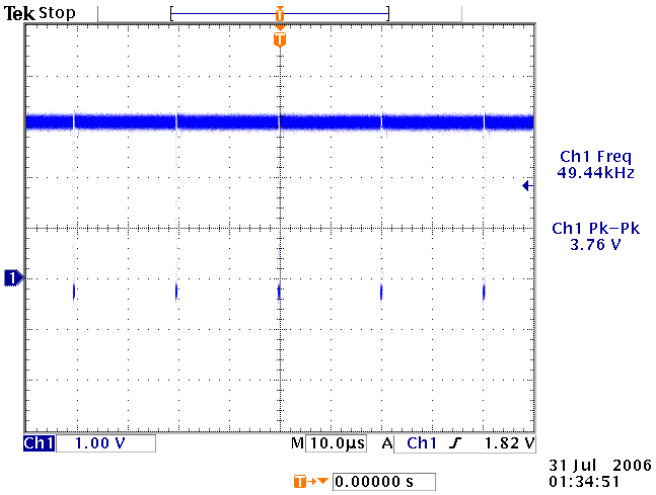
CH1 VOB0 (RP35)



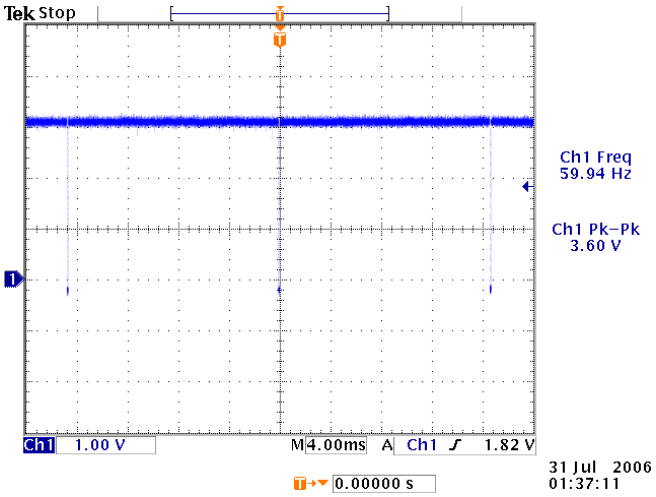
CH1 AO1MCLK (DU9 PIN J1) CH2 AO1BCK (DU9 PIN J2)



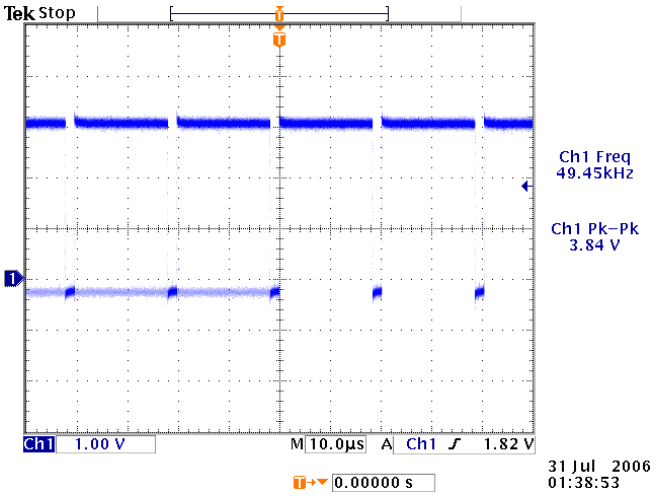
CH1 VOHSYNC (DU9 PIN V4)



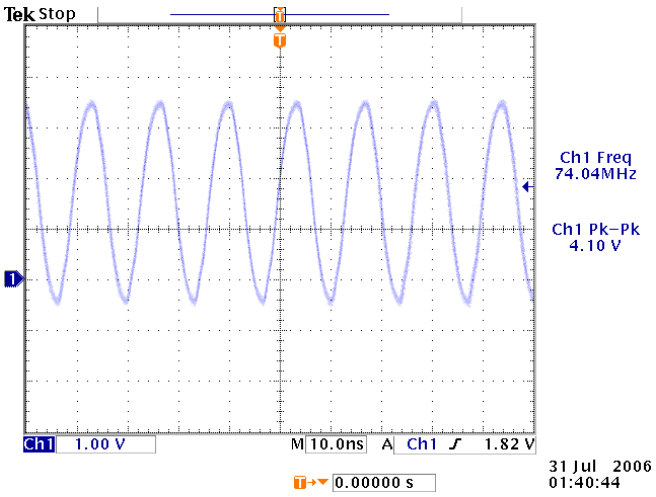
CH1 VOVSYNC (DU9 PIN W1)



CH1 VODE (DU9 PIN W2)

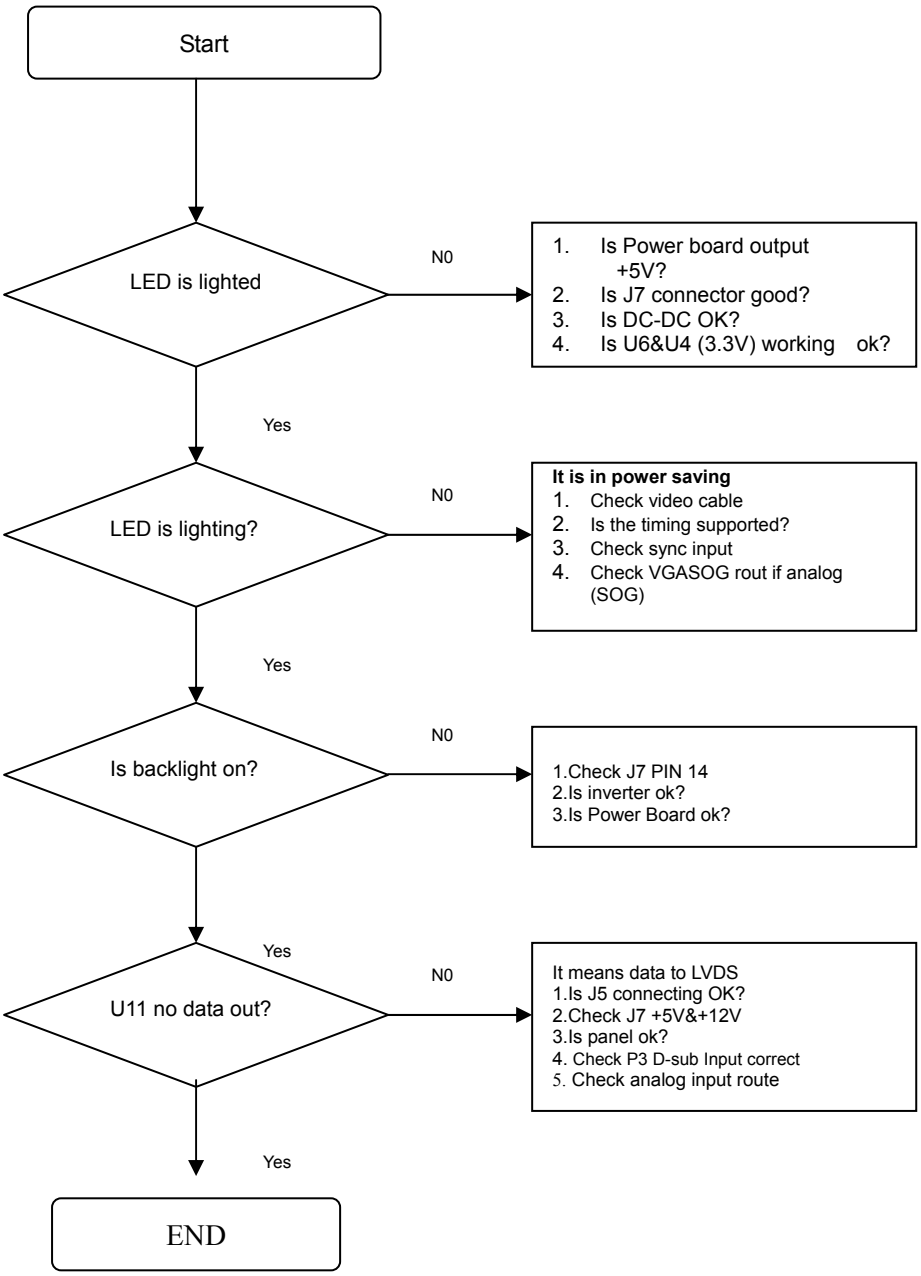


CH1 VOPCLK (DU9 PIN V3)

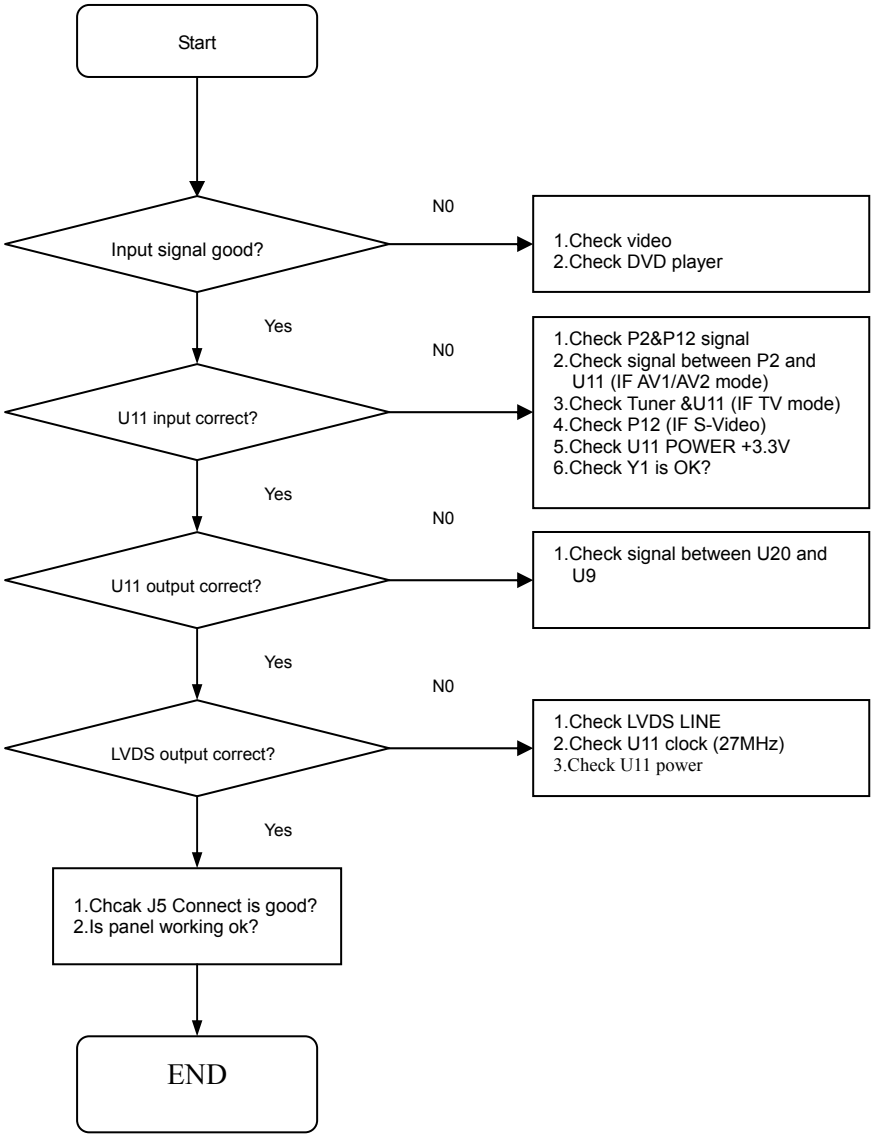


Chapter 9 Trouble shooting

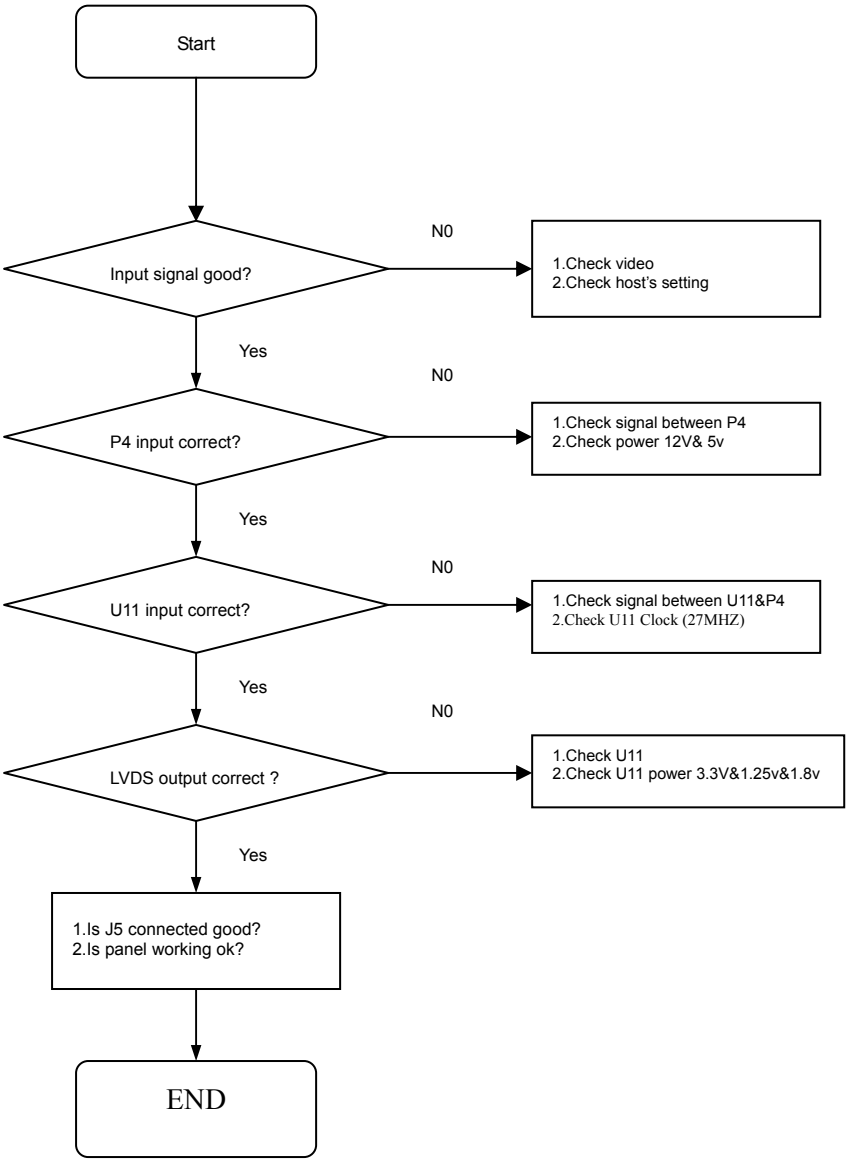
MONITOR DISPLAY NOTHING (PC MODE)



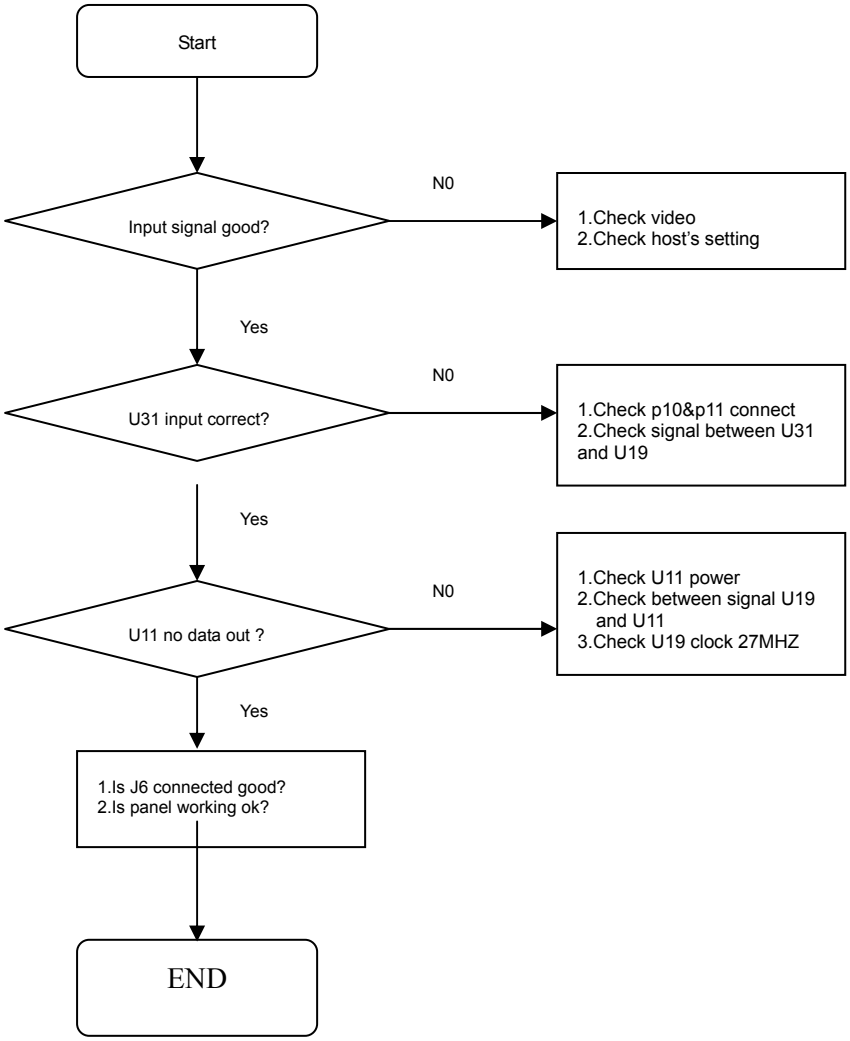
(TV, COMPOSITE VIDEO1, 2, S-VIDEO) IS NOT DISPLAY CORRECTLY



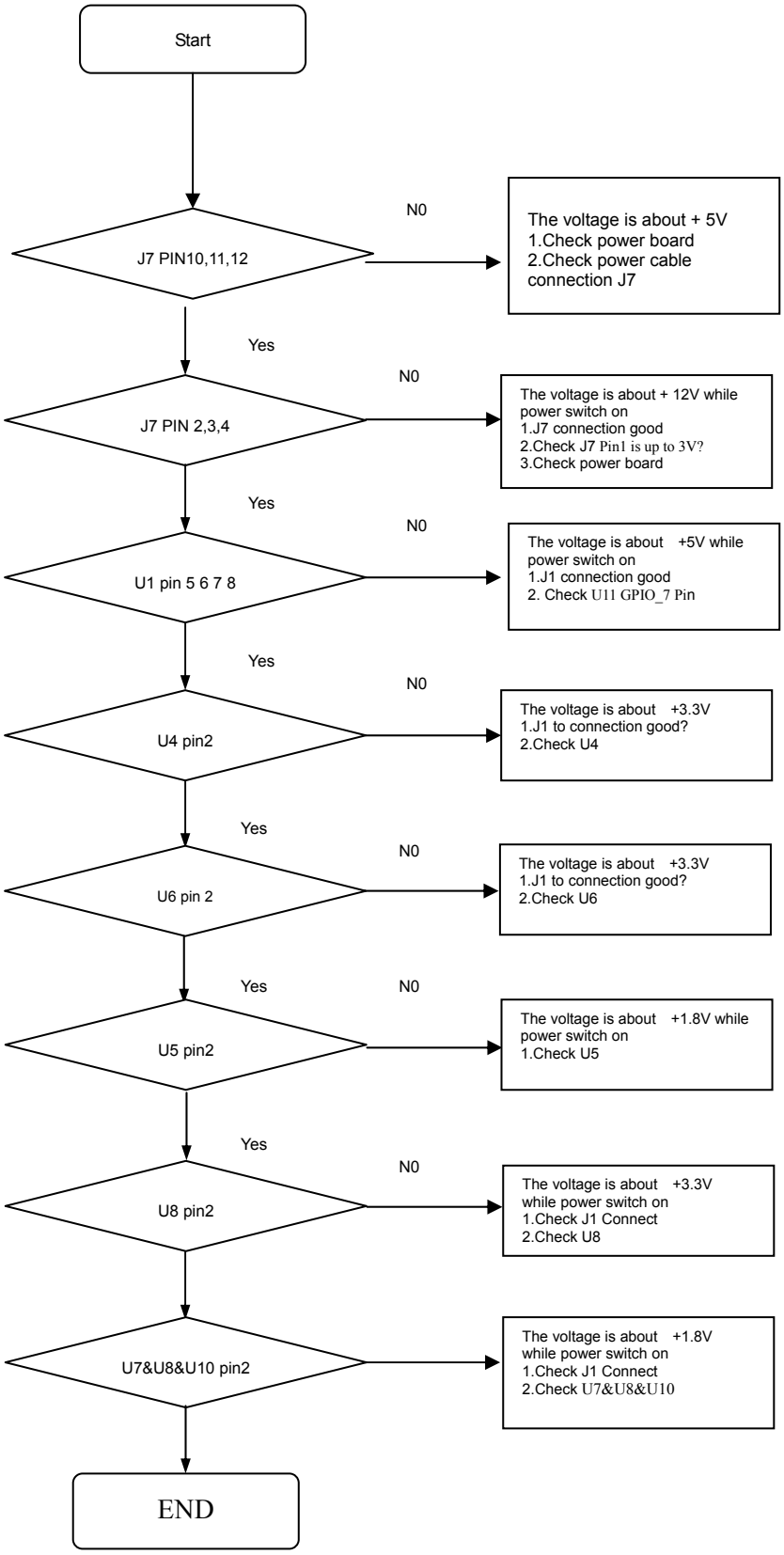
(COMPONENT1, 2) IS NOT DISPLAY CORRECTLY



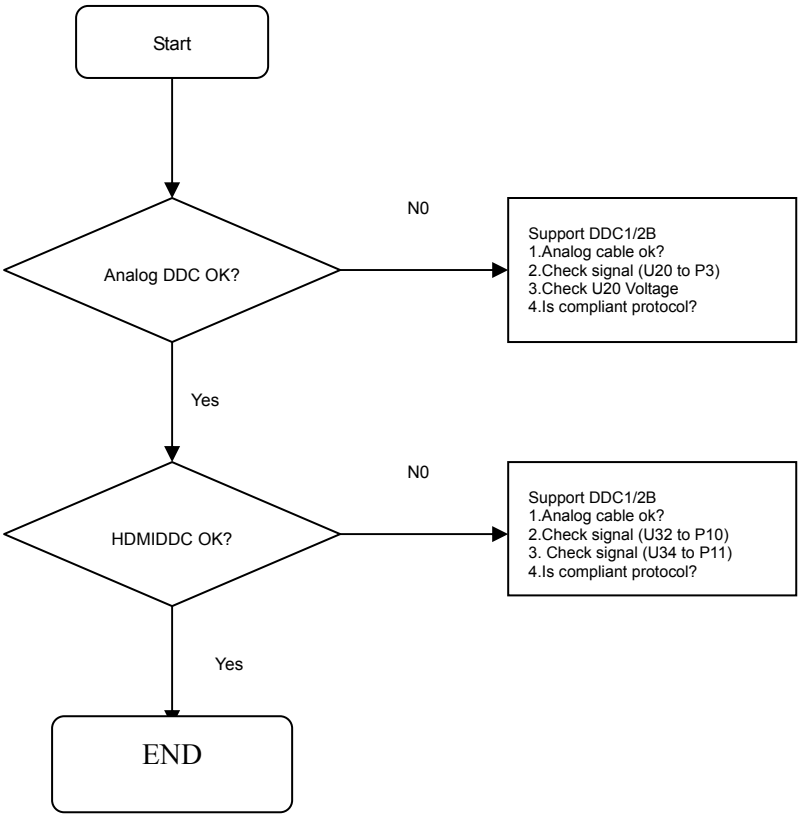
(HDMI) IS NOT DISPLAY CORRECTLY



TROUBLE OF DC-DC CONVERTER

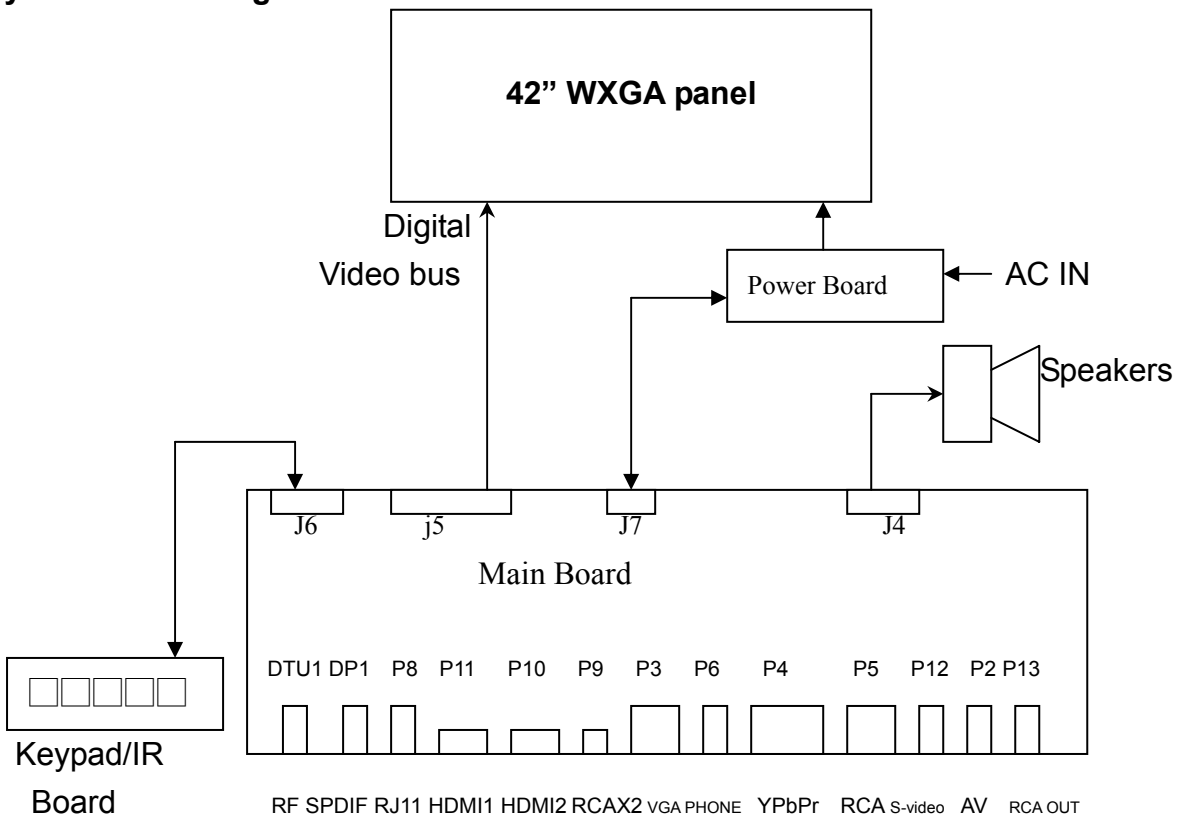


TROUBLE OF DDC READING



Chapter 10 Block Diagram

System Block Diagram

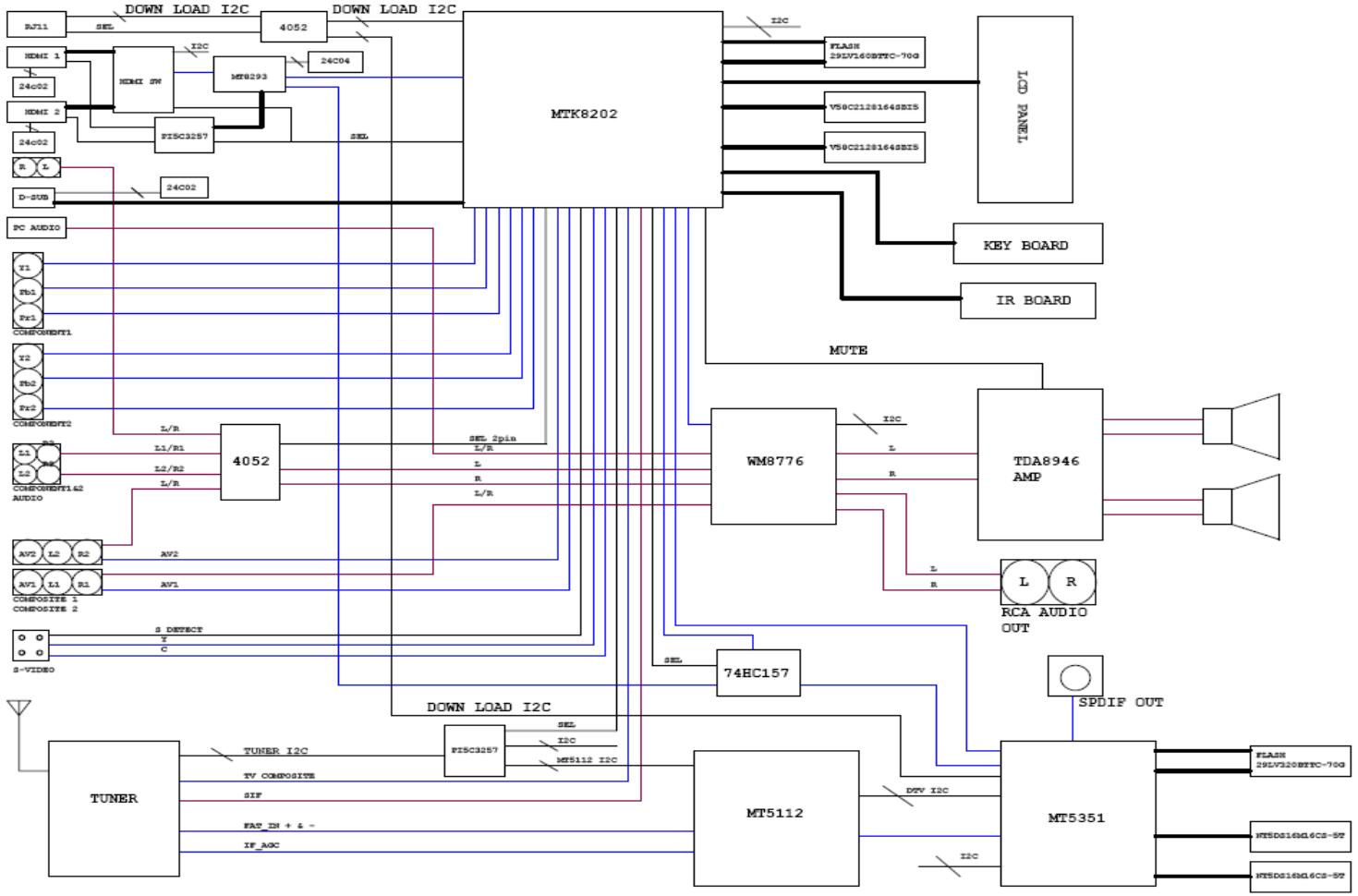


The TV system block diagram is powered by power board that transforms AC source of 100V~240V AC +/- 10% @ 50/60 HZ into DC 5V & 12V& 24Vsource. The main board receives different types of video signal into the MTK8202 Ic. Afterward, the MTK8202 Ic process the signals control the various functions of the monitor and outputs control signal, video signal and power to the 42” WXGA panel to be displayed.

The power send to the panel is first processed by the inverter. The function of the inverter is to step up the voltage supplied by the main board to the power that is needed to light up the lamps in the panel. Simultaneously, the digital video signals are processed in the panel and the outcome determines the brightness, pixel on/off and the color displayed on the panel. The analog video signals of S-video, YPbPr, TV, PC and A/V all video signals are translated from analog signals into MTK8202 generates the vertical and horizontal timing signals for display device. The analog audio of s-video, YpbPr, TV, PC and A/V is transmitting to the WM877 processed.

The purpose is process the input audio signal to control volume, bass, treble, surround, and balance. The HDMI video and audio is must transmitting to MT8293 processed then TMDS signal to the MTK8202 generates the vertical and horizontal timing signals for display device. All functions are controllable by the main board. Plus, all functions in the IC boards are programmable using I2C Bus.

Main Board Block Diagram

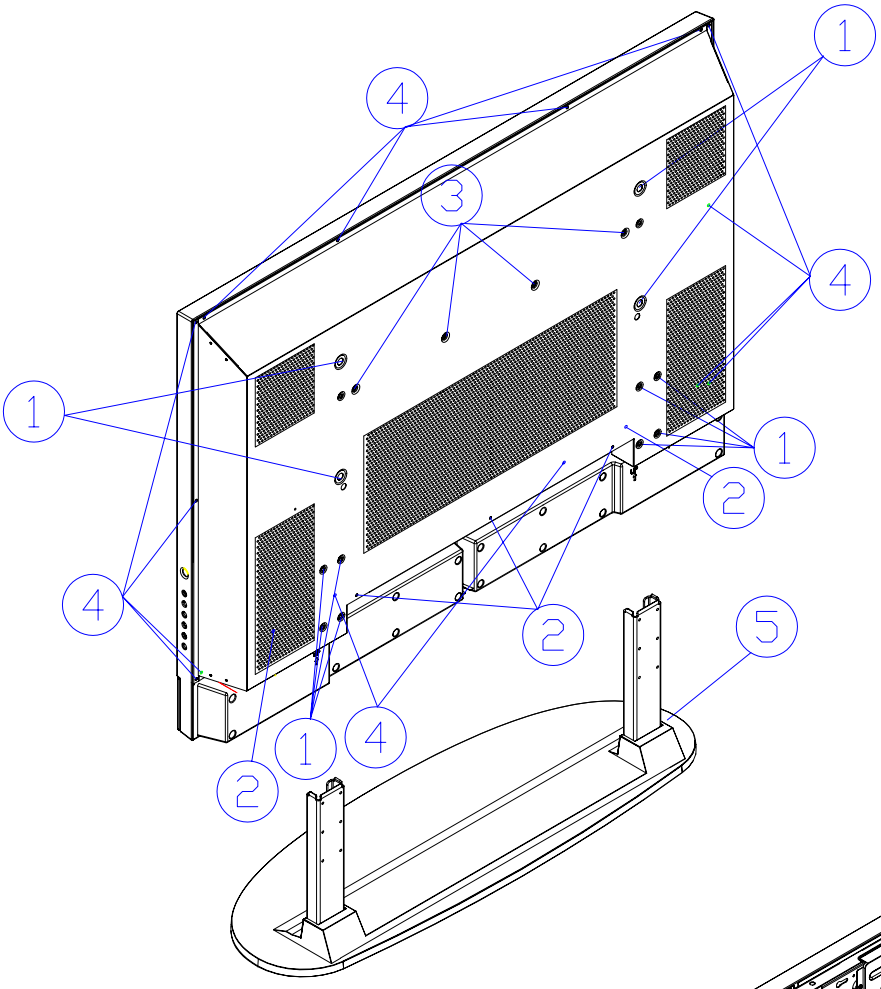


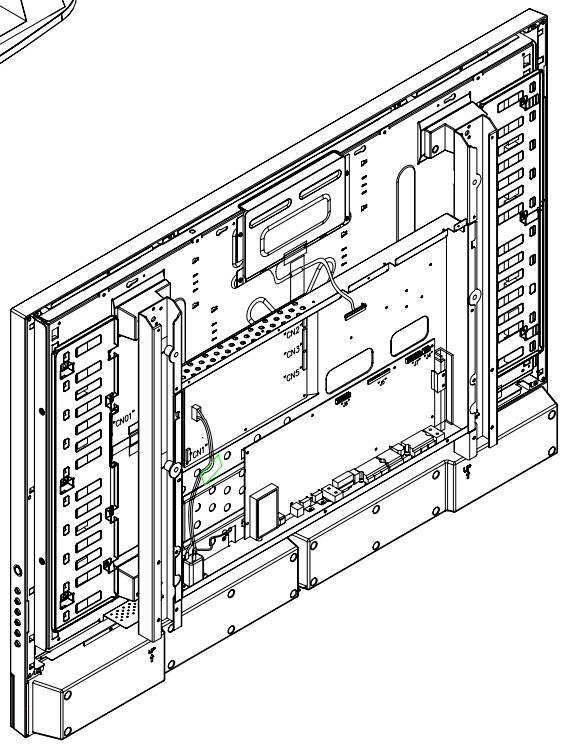
DISASSEMBLY INSTRUCTIONS

1.REAR COVER ASS'Y REMOVAL

Note:Spread a mat underneath to avoid damaging the TV surface.

1) Remove twelve screws ①from rear cover.
2) Separate the Base Ass'y⑤.
3) Remove five screws ②and four screws ③and fourteen screws ④from rear cover.
4) Separate the rear cover.

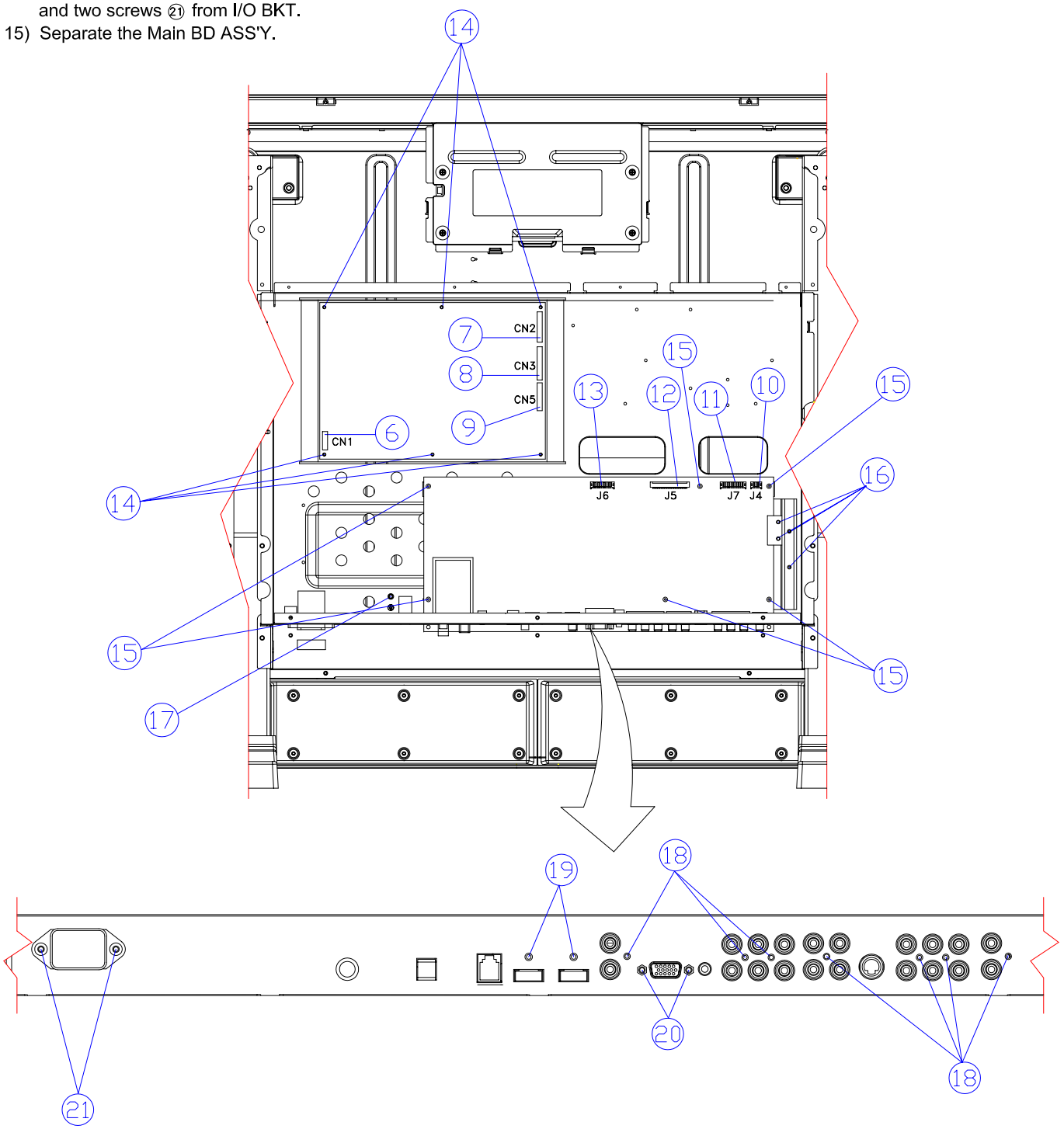




DISASSEMBLY INSTRUCTIONS

1.MAIN SD ASS'Y / POWER ASS'Y REMOVAL

1) Remove the connector ⑥ (CN1) of the AC power cable.
2) Remove the connector ⑦ (CN2) of the Inventer cable.
3) Remove the connector ⑧ (CN3) of the Inventer cable.
4) Remove the connector ⑨ (CN5) of the Main BD cable.
5) Remove six screws ⑭ from Power BD ASS'Y.
6) Separate the Power BD ASS'Y.
7) Remove the connector ⑩(J4) of the speaker cable.
8) Remove the connector ⑪(J7) of the Main BD cable.
9) Remove the connector ⑫(J5) of the LVDS cable.
10) Remove the connector ⑬(J6) of the display + IR BD cable.
11) Remove six screws ⑮ from Main BD ASS'Y.
12) Remove four screws ⑯ from heatsink.
13) Remove one screw ⑰ from PCB Support.
14) Remove seven screws ⑱,two screws ⑲ ,two hexagon screws ⑳ and two screws ㉑ from I/O BKT.
15) Separate the Main BD ASS'Y.



ITEM	PART NO.	DESCRIPTION	QTY
1	1701-1929-5010	SPEAKER NET(L42 HDTV10A)(HIPS,877C)	2
2	1947-1500-2890	SPONGE(146*7mm)	4
3	1947-1500-2900	SPONGE(80*7mm)	4
4	1801-0122-9010	FRONT BEZEL (L42 HDTV10A)(ABS.BLACK)ASS'Y	1
5	3420-0012-0156	DISPLAY BD ASS'Y L42 HDTV10A	1
6	1701-0416-9010	BUTTON(PD-42FBU)(ABS,Cr-plating)	1
7	3642-0012-0189	IR BD ASS'Y L42 HDTV10A	1
8	1712-0101-0440	PANEL BKT H(L42 HDTV10A_AUO)(SECC T=0.8mm)	2
9	1712-0101-0450	PANEL BKT V(L42 HDTV10A_AUO)(SECC T=0.8mm)	2
10	1947-1700-0020	SHIELDING AL. TAPE(45.0*25.0)	1
11	1947-1200-3480	NonWoven(160*7mm, t=0.35mm)	1
12	0211-0420-0777	LCD MODULE 42.0"TFT T420XW01 V0(AUO)	1
13	0460-3430-0930	WH FI-X30CXEL/P240430 20276 480mm+CORE	1
14	1701-1931-6020	FRAME ADAPTER BR(L42 HDTV10A_AUO)(ABS,NATURE)	2
15	1701-1931-6010	FRAME ADAPTER BL(L42 HDTV10A_AUO)(ABS,NATURE)	2
16	1712-0100-9850	MAIN FRAME R (L42 HDTV10A)(SECC T=2.0mm)	1
17	1712-0100-9860	MAIN FRAME L (L42 HDTV10A)(SECC T=2.0mm)	1
18	1712-0100-9891	PCB SUPPORT(L42 HDTV10A)(SECC T=0.8mm)	1
19	0260-0000-0220	AC INLET+VHR5P 1617#22 270mm 1015#18 115mm	1
20	1712-0100-9900	I/O BKT (L42 HDTV10A)(SECC T=0.8mm)	1
21	0500-0507-0230	POWER BD ASS'Y DPS-283APL-F	1
22	3642-0052-0150	MAIN BD ASS'Y L42 HDTV10A_AUO(HPFC)	1
23	1712-0400-0720	HEAK SINK(PD-42S)	1
24	1947-1900-0160	HEAT PATH (25*14mm,t=1mm)	1
25	1712-0100-4590	HEAT SINK FIX METAL(TM-30A)	1
26	0460-1014-0070	WH PH14P-A2543I2P 1007#24 600mm	1
27	0460-4013-0140	WH A2543H13P-PH12P 1007#24 600mm	1
28	0460-4015-0020	WH A2543H13P-A2001H02-14P 1007#24 340mm	1
29	0460-1008-0430	WH A2001H02-8P-A2001H02-4P+5P 246#28 980mm	1
30	0335-1006-0452	SPEAKER ASS'Y60HM 10W BOX+Wire#1100/620mmL-F	1
31	1701-1929-6010	SPEAKER REAR COVER-R (L42 HDTV10A)(HIPS,BLACK)	1
32	1701-1929-6020	SPEAKER REAR COVER-L (L42 HDTV10A)(HIPS,BLACK)	1
33	1712-0200-0450	REAR COVER(L42 HDTV10A)(SGCC T=0.8,mm)	1
34	1701-0520-2030	BASE COVER(PD-42L)(ABS,877C)	1
35	1712-0100-8981	BASE FRAME(PD-42L)(SPGC T=2.5mm)	2
36	1712-0100-8991	BASE PLATE(PD-42L)(SECC T1.2/ø 6mm)	1
37	1947-1200-3420	Masking Mylar(13*25mm,t=0.25mm)	1
38	1947-1800-0490	GASKET BLOCK(12L*10W*2.5Hmm)HOLE6ø	1
39	1947-1200-0400	ACETATE CLOTH TAPE(20*45mm)	17
40	1947-1200-0310	ACETATE CLOTH TAPE(27*75mm)	4
41	1701-1500-1080	EDGE SADDLE DS-12(NYLON)	4
42	1721-0003-0650	TAP.SCREW-WB #3.0*6.0L.BLK-Ni	9
43	1721-0003-1250	TAP.SCREW-TB#3.0*12.0L.BLK-Ni	32
44	1720-1504-4050	MAC.SCREW-WPSWF M4.0*40L.BLK-Ni	8
45	1721-4103-0820	TAP.SCREW-TRF#3.0*8.0L.Ni	6
46	1720-0003-0650	MAC.SCREW-WB M3.0*6.0L.BLK-Ni	28
47	1720-1204-0820	MAC.SCREW-WPGW M4.0*8.0L.Ni	1
48	1720-7344-0820	MAC.SCREW-WHSW #4-4.0*8.0L.Ni	2
49	1720-0004-0850	MAC.SCREW-WB M4.0*8.0L.BLK-Ni	28
50	1720-4003-0650	MAC.SCREW-WRF M3.0*6.0L.BLK-Ni	4
51	1721-3003-0920	TAP.SCREW-MF M3.0*9.0L.Ni	15
52	1701-1000-0520	FOOT(PORON)(20mm*15mm/2.0mm)(PD-42L)	8

UNLESS OTHERWISE NOTED	DSN: OLIVE CHEN	06/10/24	MATERIAL: ******
.XX = ±0.10	CHK:		QTY: 1 SIZE: A1
.X = ±0.2			SCALE: Full UNIT: MM
ANG = ±1/2°			

TECHNOLOGY Co., LTD.	THIRD ANGLE PROJECTION	MODEL No.	VIZIO L42HDTV10A(AUO)
VIZIO L42HDTV10A	DESCRIPTION		PART NO.
			9642-8500-1143

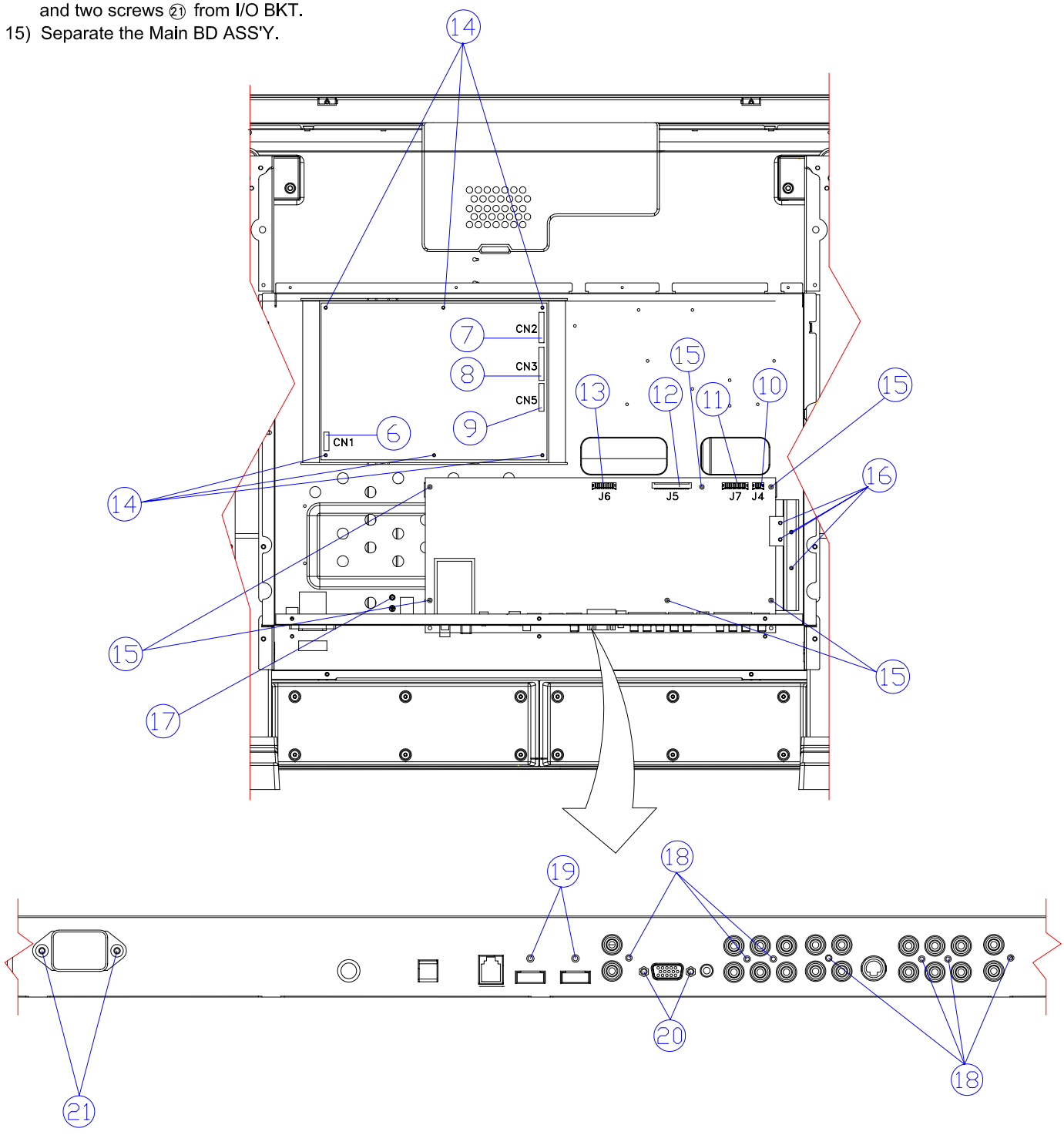
DWG. NAME: 42" CASE ASS'Y

DWG No. VIZIO-L42HDTV-10A-AUO.DRO REV. 0 SHEET: 1 of 1

DISASSEMBLY INSTRUCTIONS

1.MAIN SD ASS'Y / POWER ASS'Y REMOVAL

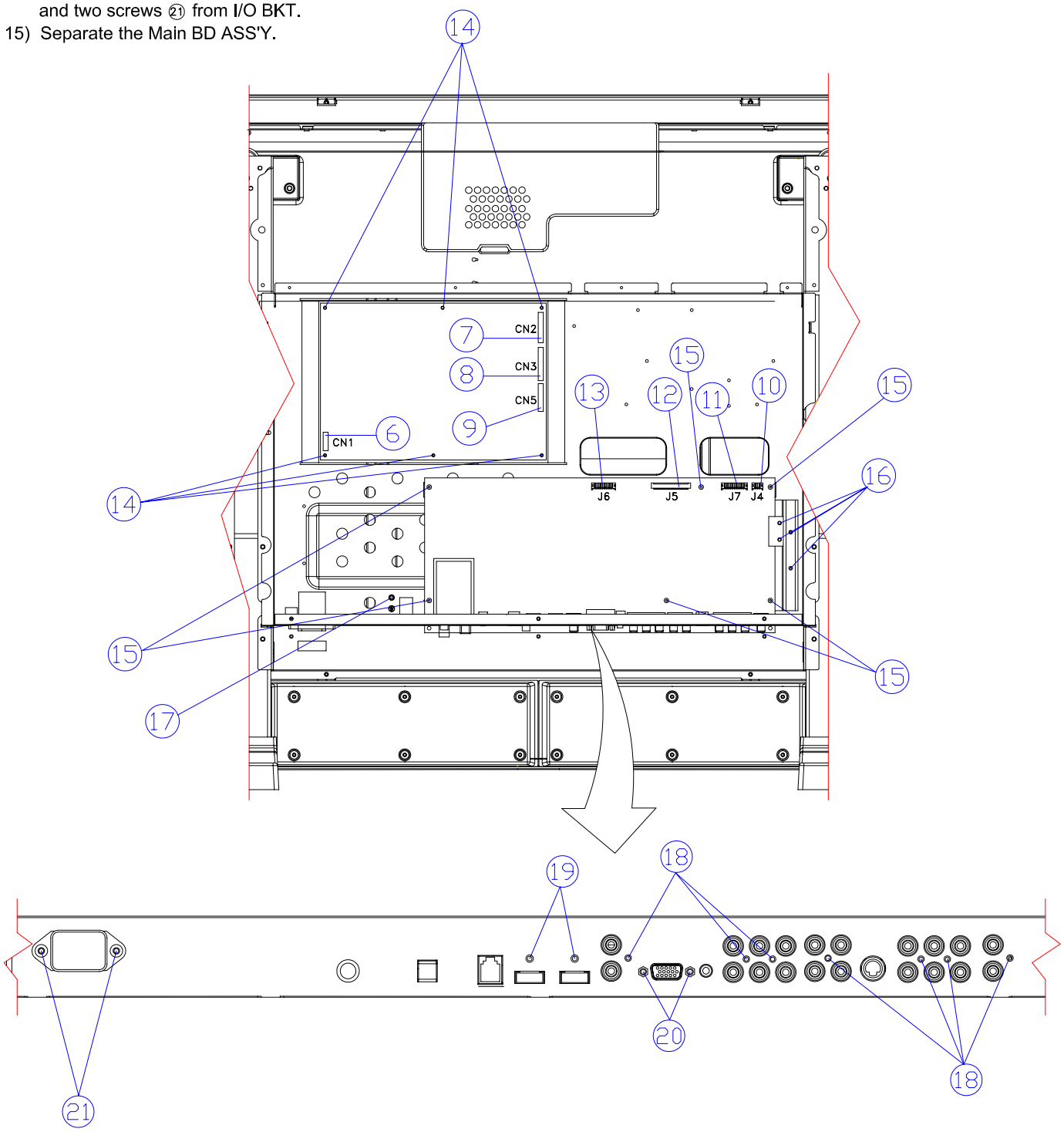
1) Remove the connector ⑥ (CN1) of the AC power cable.
2) Remove the connector ⑦ (CN2) of the Inventer cable.
3) Remove the connector ⑧ (CN3) of the Inventer cable.
4) Remove the connector ⑨ (CN5) of the Main BD cable.
5) Remove six screws ⑭ from Power BD ASS'Y.
6) Separate the Power BD ASS'Y.
7) Remove the connector ⑩ (J4) of the speaker cable.
8) Remove the connector ⑪ (J7) of the Main BD cable.
9) Remove the connector ⑫ (J5) of the LVDS cable.
10) Remove the connector ⑬ (J6) of the display + IR BD cable.
11) Remove six screws ⑮ from Main BD ASS'Y.
12) Remove four screws ⑯ from heatsink.
13) Remove one screw ⑰ from PCB Support.
14) Remove seven screws ⑱,two screws ⑲ ,two hexagon screws ⑳ and two screws ㉑ from I/O BKT.
15) Separate the Main BD ASS'Y.



DISASSEMBLY INSTRUCTIONS

1.MAIN SD ASS'Y / POWER ASS'Y REMOVAL

1) Remove the connector ⑥ (CN1) of the AC power cable.
2) Remove the connector ⑦ (CN2) of the Inventer cable.
3) Remove the connector ⑧ (CN3) of the Inventer cable.
4) Remove the connector ⑨ (CN5) of the Main BD cable.
5) Remove six screws ⑭ from Power BD ASS'Y.
6) Separate the Power BD ASS'Y.
7) Remove the connector ⑩(J4) of the speaker cable.
8) Remove the connector ⑪(J7) of the Main BD cable.
9) Remove the connector ⑫(J5) of the LVDS cable.
10) Remove the connector ⑬(J6) of the display + IR BD cable.
11) Remove six screws ⑮ from Main BD ASS'Y.
12) Remove four screws ⑯ from heatsink.
13) Remove one screw ⑰ from PCB Support.
14) Remove seven screws ⑱,two screws ⑲ ,two hexagon screws ⑳ and two screws ㉑ from I/O BKT.
15) Separate the Main BD ASS'Y.



ITEM	PART NO.	DESCRIPTION	QTY
1	1701-1929-5010	SPEAKER NET(L42 HDTV10A)(HIPS,877C)	2
2	1947-1500-2890	SPONGE(146*7mm)	4
3	1947-1500-2900	SPONGE(80*7mm)	4
4	1801-0122-9010	FRONT BEZEL (L42 HDTV10A)(ABS.BLACK)ASS'Y	1
5	3420-0012-0156	DISPLAY BD ASS'Y L42 HDTV10A	1
6	1701-0416-9010	BUTTON(PD-42FBJ)(ABS,Cr-Plating)	1
7	3642-0012-0189	IR BD ASS'Y L42 HDTV10A	1
8	1712-0100-9870	PANEL BKT H(L42-AB)(SECC T=0.8mm)	2
9	1712-0100-9880	PANEL BKT V(L42 HDTV10A)(SECC T=0.8mm)	2
10	1947-1700-0020	SHIELDING AL. TAPE(45.0*25.0)	1
11	1947-1200-3480	NonWoven(160*7mm, t=0.35mm)	1
12	0122-0420-0661	LCD MODULE 42.0"TFT LC420WO2-SLA1(LG.PHILIP)	1
13	0460-3430-0890	WH FI-X30C2EL/P2404430 20276 480mm+CORE	1
14	1701-1929-7010	FRAME ADAPTER BR(L42 HDTV10A)(ABS,NATURE)	2
15	1701-1929-7020	FRAME ADAPTER BL(L42 HDTV10A)(ABS,NATURE)	2
16	1712-0100-9850	MAIN FRAME R (L42 HDTV10A)(SECC T=2.0mm)	1
17	1712-0100-9860	MAIN FRAME L (L42 HDTV10A)(SECC T=2.0mm)	1
18	1712-0100-9891	PCB SUPPORT(L42 HDTV10A)(SECC T=0.8mm)	1
19	0260-0000-0220	AC INLET+VHR5P 1617#22 270mm 1015#18 115mm	1
20	1712-0100-9900	I/O BKT (L42 HDTV10A)(SECC T=0.8mm)	1
21	0500-0507-0230	POWER BD ASS'Y DPS-283APL-F	1
22	3642-0062-0150	MAIN BD ASS'Y L42 HDTV10A_LGHDPC)	1
23	1712-0400-0720	HEAK SINK(PD-42S)	1
24	1947-1900-0160	HEAT PATH (25*14mm,t=1mm)	1
25	1712-0100-4590	HEAT SINK FIX MTEAL(TM-30A)	1
26	0460-4013-0110	WH A2543H13P-A2001H02-12P 1007#24 600mm	2
27	1947-1800-0490	GASKET BLOCK(12L*10W*2.5Hmm)HOLE6ø	1
28	0460-4015-0020	WH A2543H15P-A2001H02-14P 1007#24 340mm	1
29	0460-1008-0430	WH A2001H02-8P-A2001H02-4P+5P 246#28 980mm	1
30	0335-1006-0452	SPEAKER ASS'Y60HM 10W BOX+Wire1100/620mmL-F	1
31	1701-1929-6010	SPEAKER REAR COVER-R (L42 HDTV10A)(HIPS,BLACK)	1
32	1701-1929-6020	SPEAKER REAR COVER-L (L42 HDTV10A)(HIPS,BLACK)	1
33	1712-0200-0450	REAR COVER(L42 HDTV10A)(SGCC T=0.8,mm)	1
34	1701-0520-2030	BASE COVER(PD-42L)(ABS,877C)	1
35	1712-0100-8981	BASE FRAME(PD-42L)(SPGC T=2.5mm)	2
36	1712-0100-8991	BASE PLATE(PD-42L)(SECC T1.2/ø 8mm)	1
37	1947-1200-3420	Masking Mylar(13*25mm,t=0.25mm)	1
38	1947-1200-0400	ACETATE CLOTH TAPE(20*45mm)	14
39	1947-1200-0310	ACETATE CLOTH TAPE(27*75mm)	4
40	1701-1500-1080	EDGE SADDLE DS-12(NYLON)	4
41	1701-1000-0520	FOOT(PORON)(20mm*15mm/2.0mm)(PD-42L)	8
42	1721-0003-0650	TAP.SCREW-TB #3.0*6.0L.BLK-Ni	9
43	1721-0003-1250	TAP.SCREW-TB#3.0*12.0L.BLK-Ni	32
44	1720-1504-3520	MAC.SCREW-MPSWF M4.0*35.0L.Ni	8
45	1721-4103-0820	TAP.SCREW-TRF#3.0*8.0L.Ni	6
46	1720-0003-0650	MAC.SCREW-MB M3.0*6.0L.BLK-Ni	28
47	1720-1204-0820	MAC.SCREW-MPOW M4.0*8.0L.Ni	1
48	1720-7344-0820	MAC.SCREW-WHSW #4-4.0*8.0L.Ni	2
49	1720-0004-0650	MAC.SCREW-MB M4.0*8.0L.BLK-Ni	28
50	1720-4003-0650	MAC.SCREW-MRF M3.0*6.0L.BLK-Ni	4
51	1721-3003-0920	TAP.SCREW-MF M3.0*9.0L.Ni	15

UNLESS OTHERWISE NOTED	DSN. OLIVE CHEN	06/10/26	MATERIAL: ******
.XX = ±0.10	CHK.		QTY. 1
.X = ±0.2			SIZE: A1
ANG. = ±1/2°			SCALE: Full UNIT: MM

TECHNOLOGY Co., LTD

THIRD ANGLE PROJECTION

VIZIO L42HDTV10A(LC)

MODEL No.

VIZIO L42HDTV10A

9642-B500-1053

PART NO.

42" CASE ASS'Y

DWG. NAME:

VIZIO-LABHDTV 10A-LC.DWG

DWG. No.

REV. 0

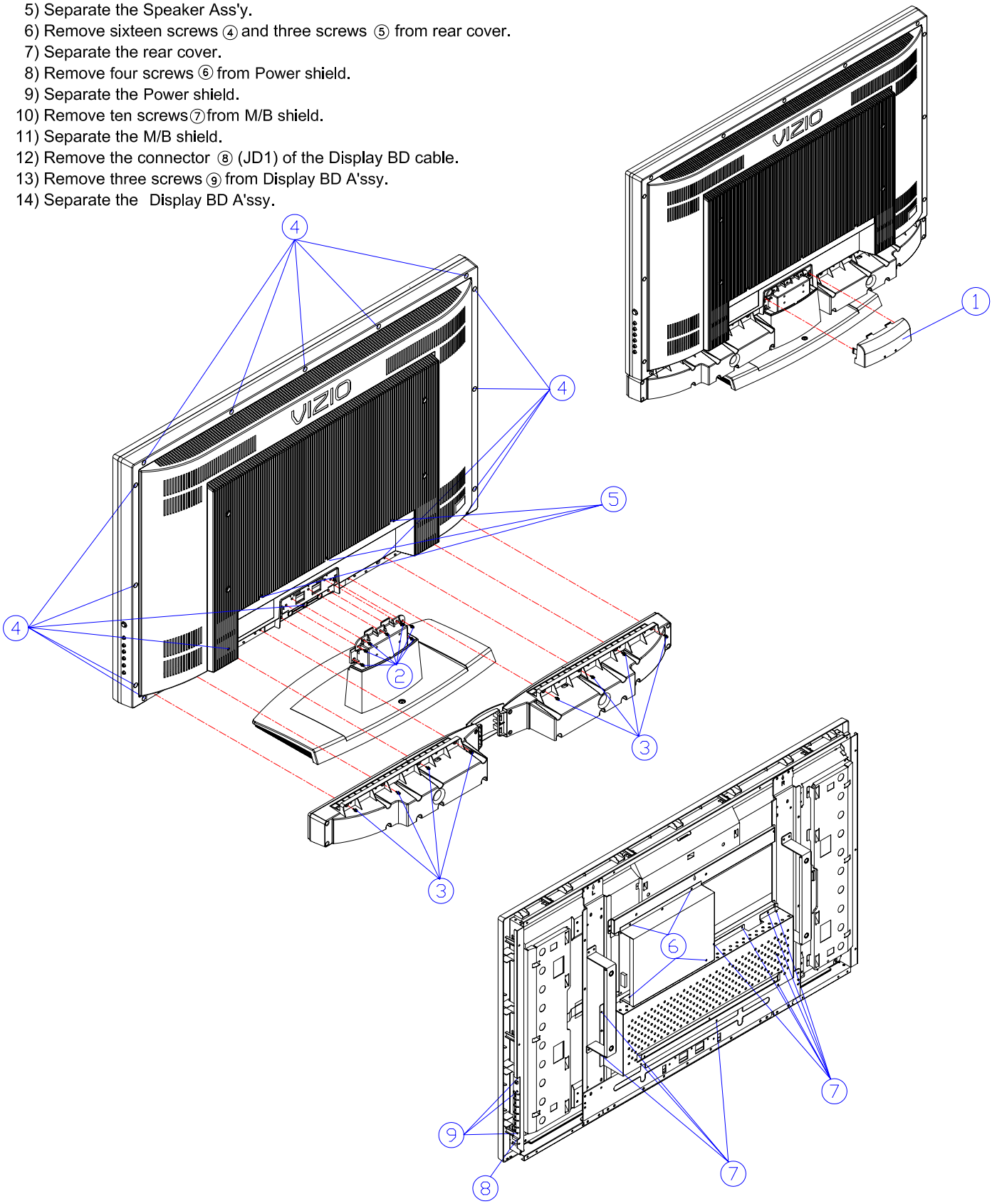
SHEET: 1 of 1

DISASSEMBLY INSTRUCTIONS

1.REAR COVER ASS'Y REMOVAL

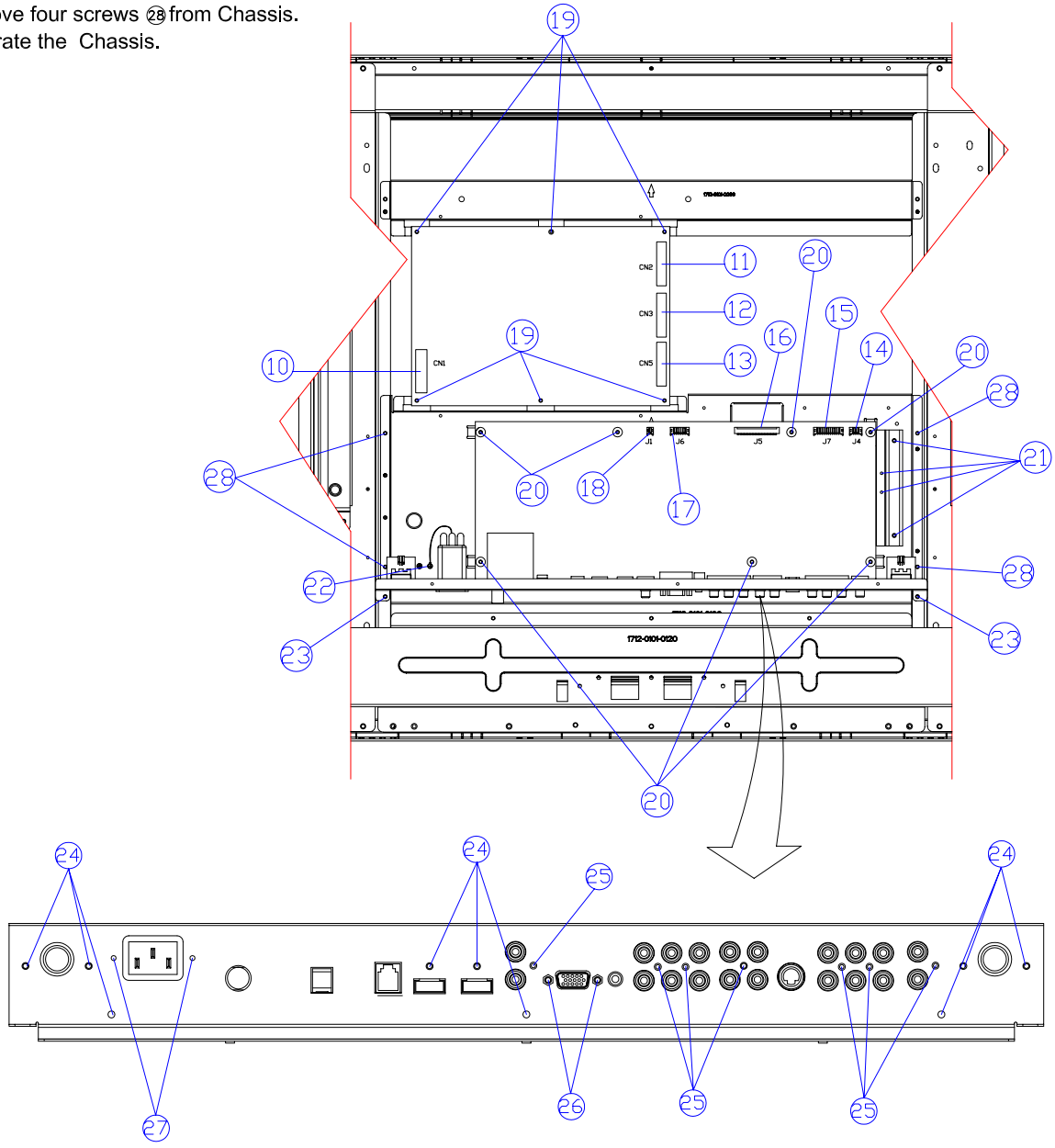
Note:Spread a mat underneath to avoid damaging the Plasma surface.

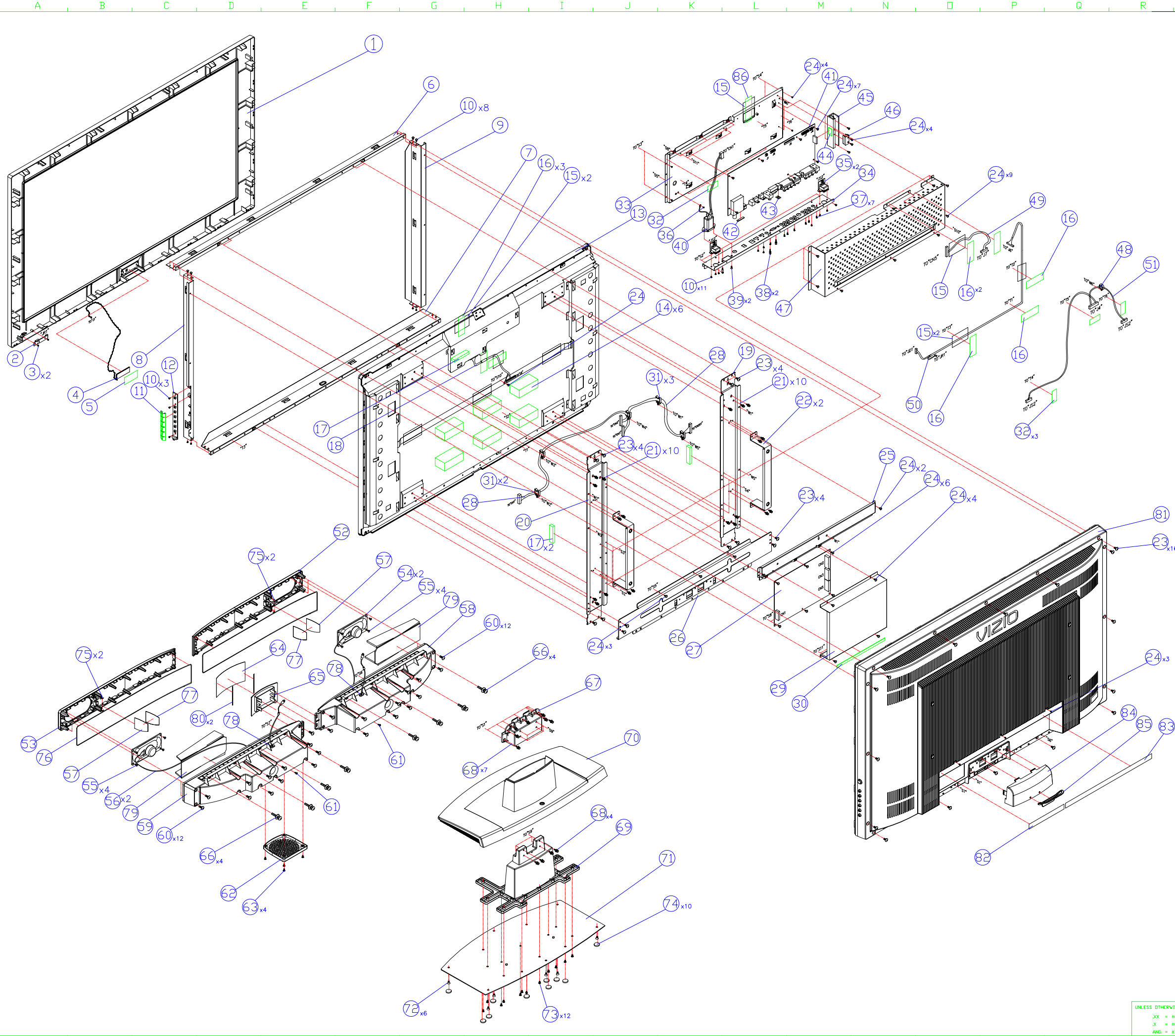
1) Separate the Base cover ①from rear cover.
2) Remove seven screws ② from Base Ass'y.
3) Separate the Base Ass'y.
4) Remove eight screws ③from Speaker Ass'y.
5) Separate the Speaker Ass'y.
6) Remove sixteen screws ④ and three screws ⑤ from rear cover.
7) Separate the rear cover.
8) Remove four screws ⑥ from Power shield.
9) Separate the Power shield.
10) Remove ten screws ⑦from M/B shield.
11) Separate the M/B shield.
12) Remove the connector ⑧ (JD1) of the Display BD cable.
13) Remove three screws ⑨ from Display BD A'ssy.
14) Separate the Display BD A'ssy.



2.MAIN BD ASS'Y / POWER BD ASS'Y REMOVAL

1) Remove the connector ⑩ (CN1) of the AC power cable.
2) Remove the connector ⑪ (CN2) of the Inventer cable.
3) Remove the connector ⑫ (CN3) of the Inventer cable.
4) Remove the connector ⑬ (CN5) of the Main BD cable.
5) Remove six screws ⑲ from Power BD Ass'y.
6) Separate the Power BD Ass'y.
7) Remove the connector ⑭ (J4) of the LCD connector BD cable.
8) Remove the connector ⑮ (J7) of the Main BD cable.
9) Remove the connector ⑯ (J5) of the LVDS cable.
10) Remove the connector ⑰ (J6) of the display BD cable.
11) Remove the connector ⑱ (J1) of the LED Blacklight cable.
12) Remove seven screws ⑳ from Main BD Ass'y.
13) Remove four screws ㉑ from heatsink.
14) Remove one screw ㉒ from Chassis.
15) Remove two screws ㉓ from I/O BKT.
16) Remove nine screws ㉔,seven screws ㉕,two hexagon screws ㉖ and two screws ㉗ from I/O BKT.
17) Separate the Main BD A'ssy and I/O BKT.
18) Remove four screws ㉘ from Chassis.
19) Separate the Chassis.





ITEM	PART NO.	DESCRIPTION	QTY
1	1801-0123-2010	FRONT BEZEL(GV42L HDTV)(ABS)ASS'Y	1
2	3642-0022-0189	IR BD ASS'Y(GV42L HDTV)	1
3	1721-0003-0650	TAP.SCREW-TB#3.0*6.0L,BLK-NI	2
4	0980-0700-0030	LED BACKLIGHT 18*50LYSB-4916W/SY 580mm	1
5	1947-1200-0820	ACETATE CLOTH TAPE 60*45mm	1
6	1712-0101-0030	PANEL HOLDER T(GV42L HDTV)(SECC,T=1.0mm)	1
7	1712-0101-0250	PANEL HOLDER B(GV42L HDTV)(SECC,T=1.0mm)	1
8	1712-0101-0240	PANEL HOLDER L(GV42L HDTV)(SECC,T=1.0mm)	1
9	1712-0101-0020	PANEL HOLDER R(GV42L HDTV)(SECC,T=1.0mm)	1
10	1720-0003-0420	SCREW-MB M3.0*4.0L,Ni	22
11	1947-1200-3461	INSULATOR FOR KEY BD(GV42L HDTV)	1
12	3642-0012-0156	DISPLAY BD ASS'Y GV42L HDTV	1
13	0211-0420-0661	LCD MODULE42.0"TFT LC420W02-SLA1(LG.PHILIPS)	1
14	1947-1800-1040	GASKET BLOCK 17W*30H*80Lmm	6
15	1947-1700-0130	SHIELDING AL. TAPE(70.0*50.0)	6
16	1947-1200-0310	ACETATE CLOTH TAPE(27*75mm)	8
17	1947-1700-0260	GASKET BLOCK (10.0*10.5*60.0mm)	3
18	0460-3430-0910	WH FI-X30C2EL/P240430 20276 370mm+CORE+GND	1
19	1712-0101-0040	REAR BRACKET R(GV42L HDTV)(SECC,T=2.0mm)	1
20	1712-0101-0050	REAR BRACKET L(GV42L HDTV)(SECC,T=2.0mm)	1
21	1720-1504-1020	SCREW MPSWF M4.0-0.7*10.0L,Ni	20
22	1712-0101-0060	WALL MOUNT SUPPORT(GV42 HDTV)(SECC,T=2.0mm)	2
23	1720-0004-0820	MAC.SCREW-MB M4.0*8.0L,Ni	28
24	1720-0003-0650	SCREW-MB M3.0*6.0LBLK-Ni	43
25	1712-0101-0090	PCB SUPPORT TOP(GV42L HDTV)(SECC,T=1.0mm)	1
26	1712-0101-0120	STIFFENER(GV42L HDTV)(SECC,T=2.0mm)	1
27	0500-0507-0201	POWER BD ASS'Y DPS-283AP AL-F	1
28	0460-4013-0120	WH A2543H0-13-A2001H02-12P 1007#24 690mm	2
29	1712-0200-0460	POWER SHIELD(GV42L HDTV)(SGCC,T=0.5mm,BLK)	1
30	1947-1800-1050	GASKET BLOCK 10.0W*25.0L*2.0H	1
31	1701-1500-0690	WIRE SADDLE(CH-14)	5
32	1947-1200-0400	ACETATE CLOTH TAPE 20*45mm	4
33	1712-0101-0300	CHASSIS(GV42L HDTV)(SGCC,T=0.5mm)	1
34	1712-0101-0110	TERMINAL BRACKET(GV42L HDTV)(SECC,T=1.0mm)	1
35	3642-0012-0146	LCD CONNECTOR BD ASS'Y(GV42L)	2
36	1720-1204-0820	MAC.SCREW-MPGW M4.0*8.0L,Ni	1
37	1721-0003-0820	TAP.SCREW-TB#3.0*8.0L,Ni	7
38	1720-7344-0820	MAC.SCREW-MHSW #4-40*8.0L,Ni	2
39	1720-3003-0820	MAC.SCREW-MF M3.0*8.0L,Ni	2
40	0260-0000-0330	AC INLET+VHR5P 1617#22 290mm 1015#18 50mm	1
41	3642-0012-0150	MAIN BD ASS'Y GV42L HDTV (HDCP)	1
42	1947-1800-0370	GASKET BLOCK(5.5H*10.0W*30.0Lmm)	1
43	1947-1800-0490	GASKET BLOCK(12L*10W*2.5Hmm)HOLE 6 ø	1
44	1947-1900-0030	HEATPATH(25*14mm)	1
45	1712-0400-1890	HEAT SINK(GV42L HDTV)	1
46	1712-0100-4590	HEAT SINK FIX METAL(TM-30A)	1
47	1712-0101-0110	M/B SHIELD(GV42L HDTV)(SECC,T=0.8mm)	1
48	1701-1500-0450	WIRE SADDLE(CH-01P)	1
49	0460-4015-0030	WH A2543H15P-A2001H02-14P1007#24 265mm	1
50	0460-1008-0450	WH A2001H02-8P-A2001H02-4P+5P 2464#26 1050mm	1
51	0460-1104-0091	WH A2501H02-4P/A2501H02-2P+2P 1007#26 560/190 rev1	1
52	1701-0123-6031	SPEAKER FRONT COVER L (GV42/46)(ABS HB)	1
53	1701-0123-5031	SPEAKER FRONT COVER R (GV42/46)(ABS HB)	1
54	0335-1008-0090	SPEAKER ASS'Y 8OHM 10W	2
55	1721-0004-0850	TAP.SCREW-TB#4.0*8.0L,BLK-NI	8
56	0321-0200-0020	DIN5P-P2125402 2464#22 480mm 2C+S	2
57	1701-1930-9030	WOOFER ISOLATED SHEET(GV42 HDTV)	2
58	1701-0214-5010	SPEAKER REAL COVER L(GV42 HDTV)(HIPS)	1
59	1701-0214-4010	SPEAKER REAL COVER R(GV42 HDTV)(HIPS)	1
60	1721-0003-1420	TAP.SCREW-TB#3.0*14.0L,Ni	24
61	1721-0003-0850	TAP.SCREW-TB#3.0*8.0L,BLK-NI	2
62	1701-1930-8030	WOOFER COVER(GV42/46)(ABS HB)	1
63	1721-0004-1020	TAP.SCREW-TP#4.0*10.0L,Ni	4
64	1712-0300-1530	AL PLATE(GV42L HDTV)	1
65	1701-1931-0030	AL PLATE SUPPORT(GV42L HDTV)(ABS HB)	1
66	1720-1504-1821	MAC.SCREW-MPSWF M4.0*18.0L,Ni,WASHER DIA 10MM	8
67	1712-1200-0310	STAND HEAD(GV42L HDTV)(DIE Casting)	1
68	1720-1504-1550	MAC.SCREW-MPSWF M4.0*15.0L,BLK-NI	11
69	1712-1200-0301	STAND FOOT(GV42L HDTV)(DIE CASTING)	1
70	1701-0523-3010	BASE(GV42L HDTV)(ABS)	1
71	1712-0101-0010	BASE PLATE(GV42L HDTV)(SECC,T=2.0mm)	1
72	1721-3004-0820	TAP.SCREW-TR#4.0*8.0L,Ni	6
73	1720-8004-1050	MAC.SCREW,Fate Head Hexagon Bit,M4.0*10.0L BLK	12
74	1701-1000-0180	BASE FOOT(ø18.0*2.0t,PORON)	10
75	1947-1500-2870	WOOFER BLOCK SEAL(GV42L/GV46L HDTV)	4
76	1947-2000-1260	RUBBER SEAL(GV42L/GV46L HDTV)	2
77	1947-1500-2860	WOOFER ISOLATED SHEET SEAL(GV42L/GV46L HDTV)	2
78	1701-1100-1350	SPEAKER CABLE SEAL(ø4.5mm/Pantone 430C)	2
79	1947-1500-2810	2X5 SPEAKER STUFFING(GV42L/GV46L HDTV)	2
80	1947-1500-2910	AL PLATE STUFFING(GV42L HDTV)	2
81	1801-0124-2010	REAR COVER(GV42L HDTV)(ABS)ASS'Y	1
82	1701-0800-2030	REAR PLATE L VIZIO(GV42L HDTV)	1
83	1701-0800-2040	REAR PLATE R VIZIO(GV42L HDTV)	1
84	1701-0523-4010	BASE COVER(GV42L HDTV)(ABS)	1
85	1701-1500-1430	CABLE CLIP(GV42L HDTV)	1
86	1947-1200-0460	ACETATE CLOTH TAPE 27*90mm	1

VIZIO GV42 HDTV			2642-8500-2053
DESCRIPTION			PART NO.
AmTRAN TECHNOLOGY Co., LTD.		THIRD ANGLE PROJECTION	MODEL NO.: VIZIO GV42 HDTV
UNLESS OTHERWISE NOTED .XX = ±0.10 .X = ±0.2 ANG. = ±1/2°	DSN.: Olive Chen 95/10/03	MATERIAL: ●●●●●●	DWG. NAME: 42 CASE ASS'Y
	CHK.:	QTY: 1 SIZE: A1	
		SCALE: Full UNIT: MM	DWG. NO.: VIZIO GV42L HDTV-LG-CLDTC REV.: 0 SHEET: 1 of 1